

# FORESEE

## Industrial SD Datasheet

FC8MC0032G-I

FC8ME0064G-I

FC8ME0128G-I

FC8ME0256G-I

FC8ME0512G-I

Version: 1.3

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## Revision History

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1.1	2021/06/16	Modify User Capacity information.	Xuan.Chen
1.2	2022/01/14	Update 32GB product actual capacity information.	Xuan.Chen
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# 1 INTRODUCTION

## 1.1 General Description

The SD is a memory card that is specifically designed to meet the security, capacity, performance and environment requirements inherent in newly emerging audio and video consumer electronic devices. The SD will include a copyright protection mechanism that complies with the security of the SDMI standard and will be faster and capable for higher Memory capacity.

The SD security system uses mutual authentication and a "new cipher algorithm" to protect from illegal usage of the card content. A none secured access to the user's own content is also available.

The SD communication is based on an advanced 9 and 8-pin interface (SD:9pin, SD:8pin) designed to operate in at maximum operating frequency of 208MHz and 2.7V ~ 3.6V operating voltage range with 2 Type signaling(1.8V & 3.3V). More detail information on the interface, and mechanical description is defined as a part of this specification.

UHS-I and High Speed mode limited on this Specification.

## 1.2 System Features

- Compliant with SD Memory Card Specifications PHYSICAL LAYER SPECIFICATION Version 6.1
  - Based on SD Memory Card Specification 3.0 compatible Test Device.
  - Bus speed support up to SDR104 (1.8V signaling, frequency up to 208MHz)
  - Bus speed support High Speed Mode for backward compatible (3.3V signaling, frequency up to 50MHz)
- Targeted for portable and stationary applications
- Memory capacity:
  - 1) Standard Capacity SD Memory Card (SDSC): Up to and including 2GB
  - 2) High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB
  - 3) Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB
- Voltage range:
  - High Voltage SD Memory Card – Operating voltage range: 2.7-3.6V
- Designed for read-only and read/write cards.
- Bus Speed Mode (using 4 parallel data lines)
  - 1) Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed
  - 2) High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25MB/sec interface speed
  - 3) SDR12: 1.8V signaling, Frequency up to 25 MHz, up to 12.5MB/sec
  - 4) SDR25: 1.8V signaling, Frequency up to 50 MHz, up to 25MB/sec
  - 5) SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
  - 6) SDR104: 1.8V signaling, Frequency up to 208 MHz, up to 104MB/sec
  - 7) DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
- Switch function command supports Bus Speed Mode and future functions
- Correction of memory field errors
- Card removal during read operation will never harm the content
- Content Protection Mechanism - Complies with highest security of SDMI standard.

- Password Protection of cards (CMD42 - LOCK\_UNLOCK)
- For SD, Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Card Detection (Insertion/Removal)
- Application specific commands
- Comfortable erase mechanism
- Global wear leveling
- Weight: SD Card Max. 2.5g

### 1.3 System Block Diagram

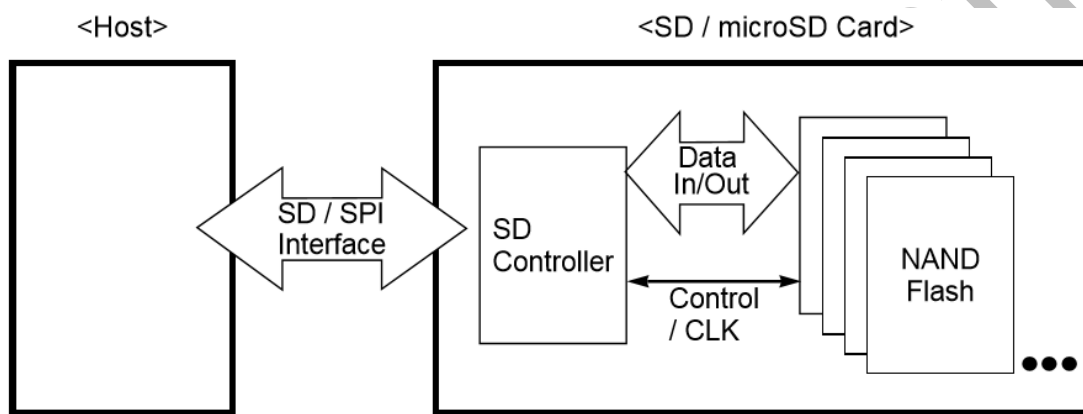


Figure 1. System Block Diagram

## 2 PRODUCT LIST

Table 1. Product Line-Up

Part Number	Capacity	Endurance	Remarks
FC8MC0032G-I	32GB	3000 Program/Erase Cycles	SDHC Card
FC8ME0064G-I	64GB	3000 Program/Erase Cycles	SDXC Card
FC8ME0128G-I	128GB	3000 Program/Erase Cycles	SDXC Card
FC8ME0256G-I	256GB	3000 Program/Erase Cycles	SDXC Card
FC8ME0512G-I	512GB	3000 Program/Erase Cycles	SDXC Card

### 3 PRODUCT SPECIFICATION

#### 3.1 Product Performance

Product Performance is based on VTE TestMetrix compliance Tool.

Note:

That the performance measured by VTE TestMetrix does not represent real performance in various circumstances.

**Table 2. Performance information**

Part Number	Sequence Write/Read (MB/S)	Speed Class
FC8MC0032G-I	Up to 30/100 MB/s	Ⓢ1 Ⓢ1 V10
FC8ME0064G-I	Up to 35/100 MB/s	Ⓢ1 Ⓢ3 V30
FC8ME0128G-I	Up to 60/100 MB/s	Ⓢ1 Ⓢ3 V30
FC8ME0256G-I	Up to 60/100 MB/s	Ⓢ1 Ⓢ3 V30
FC8ME0512G-I	Up to 60/100 MB/s	Ⓢ1 Ⓢ3 V30

Note:

Measurement based on VTE3100 & VTE4100 TestMetrix device, SW 3.2A software or up version. The card must be reformatted between each script test.

Test scripts:

SD\_Card(Spec3.0\_High&Extended-Capacity\_UHS-I and Non-UHS-I)\_Compliance [rev32A]-B87.vte

SD\_Card (Spec2.0-3.0 High&Extended-Capacity\_UHS-I) Performance-Speed (Multiple Block Sequential) [rev31M] - SDR104-With Background Data.vte;

SD\_Card (Spec3.0-4.0 HC & XC -UHS-I) SD 3.0 Speed Class (Grade 1/3) [rev32A].vte

SD [Spec 5.1\_HC&XC\_UHS-I] Speed Class (Grade 1) & VSC\_6\_10\_30 [VTE4100, Rail\_UHS-I+II] SK1 [5.2.0.2-52B-A05].vte

### 3.2 User Capacity

This information table below provides user capacity of FORESEE SD Card. Product user density is based on SD Formatter 4.0 tool with FAT File system. SD Formatter 4.0 software formats all SD Cards and SDHC Cards using a formatting program that complies with official SD memory card requirements.

**Table 3. User Capacity**

Product Number	Capacity	File System	Actual Capacity <sup>1</sup>
FC8MC0032G-I	32GB	FAT32	29.5GB
FC8ME0064G-I	64GB	exFAT	58.9GB
FC8ME0128G-I	128GB	exFAT	117GB
FC8ME0256G-I	256GB	exFAT	233GB
FC8ME0512G-I	512GB	exFAT	476GB

Note1:

SDHC or SDXC Card file systems form attached with generic operating system formatting software do not comply with official SD memory card requirement and optimum performance may not be experienced.

### 3.3 System Performance

FORESEE SD Card shall complete the command within the time period defined as follows or give up and return an error message. If the host does not get any response with the given timeout it should assume that the card is not going to respond and try to recover.

All performance values in Table 4 were measured under the following conditions:

- Voltage range 2.7 to 3.6V
- Independent of card clock frequency

**Table 4. System information**

Timing	Maximum Value
Block Read Access Time	100ms
Block Write Access Time	250ms(SDSC/SDHC), 500ms(SDXC)
Initialization Time out(ACMD 41) <sup>1</sup>	1S

Note1:  
 The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

### 3.4 Current Consumption

This information table below provides current consumption of FORESEE SD Card. Current consumption is measured by averaging over 1 second.

**Table 5. Current Consumption Table**

Product Number	Capacity	Mode	Operation	Maximum Value	Typical Value
FC8MC0032G-I	32GB	Operation Current	Write/Read	140mA	100mA
		Standby Current	Standby	200uA	160uA
FC8ME0064G-I	64GB	Operation Current	Write/Read	180mA	140mA
		Standby Current	Standby	250uA	180uA
FC8ME0128G-I	128GB	Operation Current	Write/Read	220mA	160mA
		Standby Current	Standby	280uA	240uA
FC8ME0256G-I	256GB	Operation Current	Write/Read	220mA	165mA
		Standby Current	Standby	280uA	250uA
FC8ME0512G-I	512GB	Operation Current	Write/Read	220mA	165mA
		Standby Current	Standby	280uA	250uA

Note:  
 Test condition: Realtek5329 card reader (Voltage 3.3V), KEITHLEY DMM7510 DIGIT MULTIMETER.  
 Current consumption on each device can be varied by NAND Flash, controller, test conditions and Etc.

### 3.5 SD Mode Card Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

#### 3.5.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits.

**Table 6. OCR Register Definition**

OCR bit	OCR Fields Definition	OCR Value
0-3	reserved	0
4	reserved	0
5	reserved	0
6	reserved	0
7	reserved for Low Voltage Range	0
8	reserved	0
9	reserved	0
10	reserved	0
11	reserved	0
12	reserved	0
13	reserved	0
14	reserved	0
15	2.7 - 2.8	1
16	2.8 - 2.9	1
17	2.9 - 3.0	1
18	3.0 - 3.1	1
19	3.1 - 3.2	1
20	3.2 - 3.3	1
21	3.3 - 3.4	1
22	3.4 - 3.5	1
23	3.5 - 3.6	1
24 <sup>1</sup>	Switching to 1.8V Accepted (S18A)	0 or 1
25-28	reserved	0
29	UHS-II Card Status	
30	Card Capacity Status(CCS) <sup>2</sup>	---
31	Card power up status bit(busy) <sup>3</sup>	---

Note1:

S18A = 0 means voltage switch is not allowed.

S18A = 1 means Voltage switch is allowed and host issue CMD to invoke voltage switch sequence.

Note2:

This bit is set to LOW if the card has not finished the power up routine.

Note3:

This bit is valid only when the card power up status bit is set.

### 3.5.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number. It is programmed during manufacturing and cannot be changed by card hosts. The structure of the CID register is defined in the following paragraphs:

**Table 7. CID Register Fields**

Name	CID Bit	Width	Field	Type	CID Value
Manufacture ID	[127:120]	8	MID	Binary	CID Register Value can be provided by Customer Request
OEM/Application ID	[119:104]	16	OID	ASCII	
Product Name	[103:64]	40	PNM	ASCII	
Product Revision	[63:56]	8	PRV	BCD	
Product Serial Number	[55:24]	32	PSN	Binary	
Reserved	[23:20]	4	---	---	
Manufacturing Date	[19:8]	12	MDT	BCD	
CRC7 check sum	[7:1]	7	CRC	Binary	
Not used, always '1'	[0]	1	---	---	

### 3.5.3 CSD Register (CSD Version 2.0)

The following Table shows Definition of the CSD Version 2.0 for the High Capacity SD Memory Card and Extended Capacity SD Memory Card. The following sections describe the CSD and the relevant data types for the High Capacity SD Memory Card.

CSD Version 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

**Table 8. The CSD Register Fields (CSD Version 2.0)**

Name	CSD Bit	Width	Field	CSD Value	NOTE
CSD structure	[127:126]	2	CSD_STRUCTURE	01b	CSD Version 2.0
Reserved	[125:120]	6	---	---	---
Data read access-time 1	[119:112]	8	(TAAC)	0E h	1ms
Data read access-time2 in CLK cycles(NSA*100)	[111:104]	8	(NSAC)	00 h	0 cycle
Max data transfer rate	[103:96]	8	(TRAN_SPEED)	x	x
Card command classes	[95:84]	12	CCC	5B5 h	
Max. read data block length	[83:80]	4	(READ_BL_LEN)	9 h	512 Byte
Partial block read allowed	[79]	1	(READ_BL_PARTIAL)	0	
Write block misalignment	[78]	1	(WRITE_BLK_MISALIGN)	0	
Read block misalignment	[77]	1	(READ_BLK_MISALIGN)	0	

DSR implemented	[76]	1	DSR_IMP	0	
Reserve	[75:70]	6	---	---	
Device size	[69:48]	22	C_SIZE	xxxxxxh	
Reserved	[47]	1	---	0	
Erase single block enable	[46]	1	(ERASE_BLK_EN)	1	
Erase sector size	[45:39]	7	(SECTOR_SIZE)	7F h	
Write protect group size	[38:32]	7	C_SIZE	0 b	
Write protect group enable	[31]	1	---	0	
Reserved	[30:29]	2	(ERASE_BLK_EN)	0 b	
Write speed factor	[28:26]	3	(SECTOR_SIZE)	010 b	
Max. write data block length	[25:22]	4	(WP_GRP_SIZE)	9 h	512 Byte
Partial block write allowed	[21]	1	(WP_GRP_ENABLE)	0	
Reserved	[20:16]	5	---	---	
File format group	[15]	1	(FILE_FORMAT_GRP)	0	
Copy flag	[14]	1	COPY	0	
Permanent write protection	[13]	1	PERM_WRITE_PROTECT	0	
Temporary write protection	[12]	1	TMP_WRITE_PROTECT	0	
File format	[11:10]	2	(FILE_FORMAT)	0	
Reserved	[9:8]	2	---	---	
CRC	[7:1]	7	CRC	---	
Not used,always'1'	[0]	1	---	1	

### 3.5.4 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Card's special features that were configured into the given card. The size of SCR register is 64bits. The register shall be set in the factory by the SD Card manufacturer. The following table describes the SCR register content.

**Table 9. The SCR Fields**

Name	Field	Width	Cell Type	SCR-Bit	SCR Value
SCR structure	SCR_STRUCTURE	4	R	[63:60]	0x0
SD Memory Card-Spec. Version	SD_SPEC	4	R	[59:56]	0x2
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]	0 b
SD Security Support	SD_SECURITY	3	R	[54:52]	011 b
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]	0x5
Spec. Version 3.00 or Higher	SD_SPEC3	1	R	[47]	---
Extended Security Support	EX_SECURITY	4	R	[46:43]	---
Spec. Version 4.00 or higher	SD_SPEC4	1	R	[42]	---
Spec. Version 5.00 or higher	SD_SPECX	4	R	[41:38]	---
Reserved		2	R	[37:36]	---
Command Support bits	CMD_SUPPORT	4	R	[35:32]	---
Reserved for manufacturer usage		32	R	[31:0]	---

### 3.5.5 SD Status Register

The SD Status contains status bits that are related to the SD Memory Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran\_state' (card is selected). SD Status structure is described in below. Unused reserved bits shall be set to 0.

**Table 10. SD Status Register**

Bits	Identifier	Type	Value	Description
511:510	DATA_BUS_WIDTH	S R	'00'=1(default) '01'=reserved '10'=4 bit width '11'=reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command
509	SECURED_MODE	S R	'0'=Not in the mode '1'=In Secured Mode	Shows if the card is in the secured mode of operation or not. (refer to "Part 3 Security Specification").
508:502	Reserved for Security Functions (Refer to Part 3 Security Specification)			
501:496	Reserved			
495:480	SD_CARD_TYPE	S R	'00xxh'=SD Memory Cards ('x'=don't care).	In the future, the 8 LSBs will be used to define different

			The following cards are currently defined: '0000h'=Regular SD RD/WR Card. '0001h'=SD ROM Card '0002h'=OTP	variations of an SD Memory Card(Each bit will define different SD Types)
479:448	SIZE_OF_PROTECTED_AREA	S R	Size of protected area	(See section 4.10.2.1)
447:440	SPEED_CLASS	S R	Speed Class of card	(See section 4.10.2.2)
439:432	PERFORMANCE_MOVE	S R	Performance of move indicated by 1[MB/s] step.	(See section 4.10.2.3)
431:428	AU_SIZE	S R	Size of AU	(See section 4.10.2.4)
427:424	Reserved			
423:408	ERASE_SIZE	S R	Number of AUs to be erased at a time	(See section 4.10.2.5)
407:402	ERASE_TIMEOUT	S R	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See section 4.10.2.6)
401:400	ERASE_OFFSET	S R	Fixed offset value added to erase time	(See section 4.10.2.7)
399:396	UHS_SPEED_GRADE	S R	Speed Grade for UHS mode	(See section 4.10.2.8)
395:392	UHS_AU_SIZE	S R	Size of AU for UHS mode	(See section 4.10.2.9)
391:384	VIDEO_SPEED_CLASS	S R	Video Speed Class value of the card	(See section 4.10.2.10)
383:378	reserved			
377:368	VSC_AU_SIZE	S R	AU size in MB for Video Speed Class	(See section 4.10.2.11)
367:346	SUS_ADDR	S R	Suspension Address	(See section 4.10.2.12)
345:340	reserved			
339:336	APP_PERF_CLASS	S R	Application Performance Class Value of the card	(See section 4.10.2.13)
335:328	PERFORMANCE_ENHANCE	S R	Support for Performance Enhancement functionalities	(See section 4.10.2.14)
327:314	reserved			
313	DISCARD_SUPPORT	S R	'0' Not Supported '1' Supported	Discard Support. (See section 4.3.6)
312	FULE_SUPPORT	S R	'0' Not Supported '1' Supported	Full User Area Logical Erase Support. (See section 4.3.7)
311:0	Reserved for Manufacturer			

### 3.6 SPI Mode Card Registers

Unlike the SD Memory card protocol (where the register contents is sent as command response), reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by data block of 16 bytes suffixed with a 16bit CRC. The data timeout for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore, the standard response timeout value(NCR) is used for read latency of the CSD register.

## 4 RELIABILITY AND DURABILITY

### 4.1 Absolute Maximum Temperature Rating

Table 11. Maximum Temperature Rating

Item	Symbol	Parameter	MIN	MAX
1	Ta	Operating Temperature	-25°C	+85°C
2	Tst	Storage Temperature	-40°C	+85°C

### 4.2 Supply Voltage Range

Table 12. Supply voltage range

Item	Symbol	Parameter	MIN	MAX
1	VDD	Operating Voltage Support	+2.7V	+3.6V
2	VSS	GND	-0.3V	+0.3V

### 4.3 Temperature and Humidity

Table 13. High Temperature

Parameter	Temperature
Operation	+85°C
Storage	+85°C

Table 14. Low Temperature

Parameter	Temperature
Operation	-25°C
Storage	-40°C

Table 15. High Humidity

Parameter	Temperature	Humidity
Operation	+25°C	95% RH
Storage	+40°C	93% RH

## 4.4 Salt Water Spray

Table 16. Salt Water Spray

Parameter	Condition
Salt Water Spray Test	3% NaCl/35C

## 4.5 X-ray Exposure

Table 17. X-ray Exposure

Parameter	Condition
X-ray Exposure Test	0.1[Gy] of medium-energy radiation (70[keV] to 140[keV], cumulative dose per year) to both sides of the card, according to ISO7816-1.

## 4.6 Drop

Table 18. Drop

Parameter	Condition
Drop Test	1.5[m] free fall

## 4.7 Bending

Table 19. Bending

Parameter	Condition
Bending Test	10[N] Center 200[mm/minute] 60[sec]

## 4.8 Torque

Table 20. Torque

Parameter	Condition
Torque Test	0.15[Nm] +/- 2.5[deg] max. 30[sec]

## 4.9 Electrostatic Discharge (ESD)

Table 21. Electrostatic Discharge

Parameter	Condition
ESD Test	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF], 330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]

## 4.10 Durability

Table 22. Durability

Parameter	Condition
Durability Test	0.4N~5N, 0.6~6 sec/cycle, 10000 cycles

## 5 SD CARD COMPARISON

Table 23. Comparing SDSC, SDHC and SDXC

Item	SDSC (Backward compatible to 2.0 host)	SDHC (Backward compatible to 2.0 host)	SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 24. Comparing UHS Speed Grade Symbols

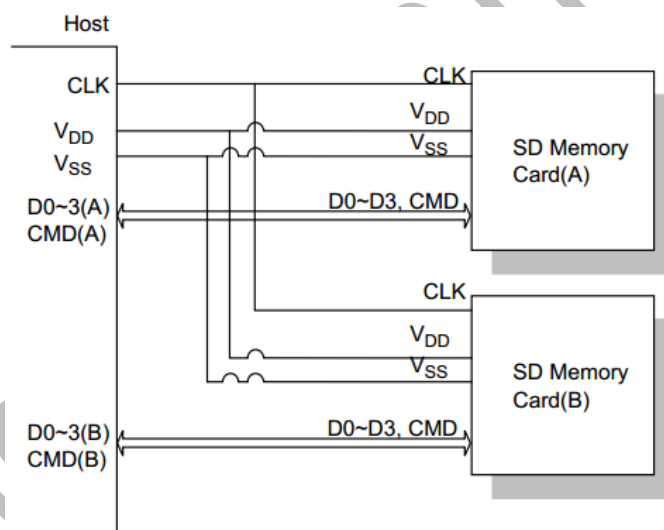
Item	U1 ( UHS Speed Grade 1)	U3 ( UHS Speed Grade 3)
Bus Mode	UHS-I /UHS-II	
SD Memory Card	SDHC, SDXC	
Mark	<b>U1</b>	<b>U3</b>
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

**Table 25. Comparing Video Speed Class Symbols**

Item	V6 (Video Speed Class 6)	V10 (Video Speed Class 10)	V30 (Video Speed Class 30)	V60 (Video Speed Class 60)	V90(Video Speed Class 90)
Bus Mode	High Speed/UHS-I/UHS-II		UHS-I/UHS-II	UHS-II	
SD Memory Card	SDHC, SDXC				
Mark	<b>V6</b>	<b>V10</b>	<b>V30</b>	<b>V60</b>	<b>V90</b>
Performance	6 MB/s minimum write speed	10 MB/s minimum write speed	30 MB/s minimum write speed	60 MB/s minimum write speed	90 MB/s minimum write speed
Applications	HD/FHD Video Recording.	FHD Video Recording HD Still Image, Continuous Shooting.		4K/2K Video Recording	8K/3D/360°Video Recording

## 6 INTERFACE DESCRIPTION

### 6.1 SD Mode Bus Topology / SPI Mode Bus Topology



**Figure 2. SD Memory Card System Bus Topology**

The SD/SD Memory Card system defines two alternative communication protocols: SD and SPI. The host system can choose either one of modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same communication mode. Common bus signals for multiple card slots are not recommended. A single SD bus should connect a single SD card. Where the host system supports a high-speed mode, a single SD bus shall be connected to a single SD card.

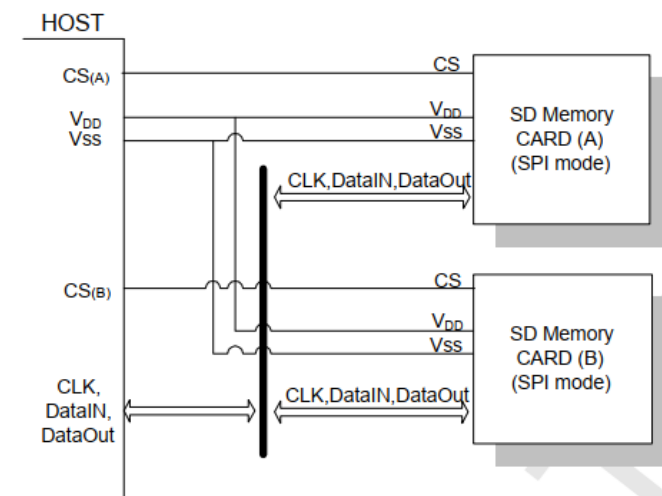
The SD/SD bus includes the following signals:

- CMD : Bidirectional Command/Response signal
- DAT0 - DAT3 : 4 Bidirectional data signals
- CLK : Host to card clock signal
- VDD, VSS1, VSS2: Power and ground signals

The SD/SD Card bus has a single master (application), multiple slaves(cards), synchronous start topology (refer to Figure 1,Figure 2 ). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process, commands are sent to each card individually allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simplify the handling of the card stack, after initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.SD Bus allows dynamic configuration of the number of data lines. After power-up, by default, the SD/SD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width(number of active data lines). This feature allows an easy tradeoff between hardware cost and system performance.

Note: that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.



**Figure 3. SD Memory Card System (SPI Mode) Bus Topology**

The SPI compatible communication mode of the SD/SD Memory Card is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.

The SPI standard defines the physical link only, and not complete data transfer protocol. The SD/SD Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD mode which enables the wide bus option.

The SD/SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the SD/SD Card SPI channel consists the following four signals:

- CS : Host to card Chip Select signal
- CLK : Host to card clock signal
- DataIN : Host to card data signal
- DataOut: Card to host data signal

Another SPI common characteristic is byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

## 6.2 Bus Protocol

### 6.2.1 SD Bus

For more details, refer to Section 3.6.1 of the SDA Physical Layer Specification, Version 6.1.

### 6.2.2 SPI Bus

For more details, refer to Chapter 7 of the SDA Physical Layer Specification, Version 6.1.

## 6.3 Pin Assignment

### 6.3.1 SD Card Assignment

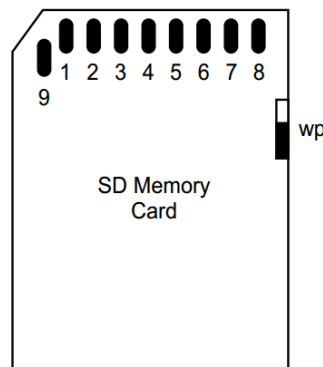


Table 26. SD Contact Pad Assignment

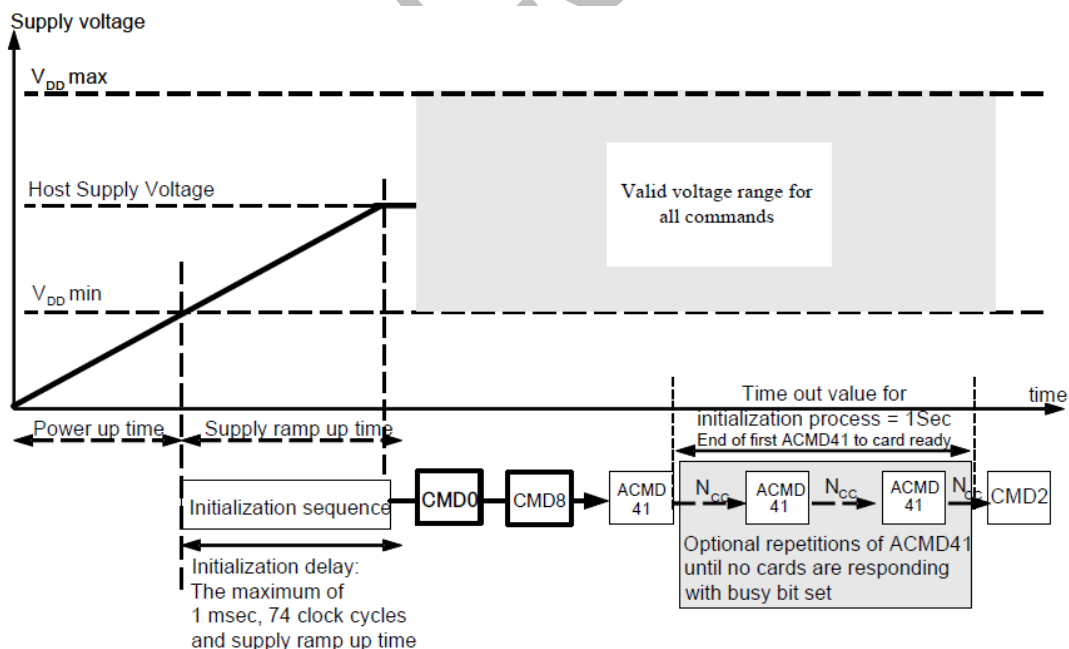
Pin	Name	Type <sup>1</sup>	Description	Pin	Name	Type	Description
SD Mode				SPI Mode			
1	CD/DAT3 <sup>2</sup>	I/O/PP3	Card Detect / Data Line [Bit 3]	1	CS	I3	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	2	DI	I	Data In
3	VSS1	S	Supply voltage ground	3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage	4	VDD	S	Supply voltage
5	CLK	I	Clock	5	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	7	DO	O/PP	Data Out
8	DAT1 <sup>4</sup>	I/O/PP	Data Line [Bit 1]	8	RSV		-
9	DAT2 <sup>5</sup>	I/O/PP	Data Line [Bit 2]	9	RSV		-

- Note1:  
 S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
- Note2:  
 The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command.  
 The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
- Note3:  
 At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection.  
 For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET\_CLR\_CARD\_DETECT (ACMD42) command
- Note4:  
 DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
- Note5:  
 DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

## 6.4 Electrical Interface

The following sections provide valuable information about the electrical interface. See Chapter 6 of the SDA Physical Layer Specification, Version 6.10 for more detail information.

### 6.4.1 Power Up



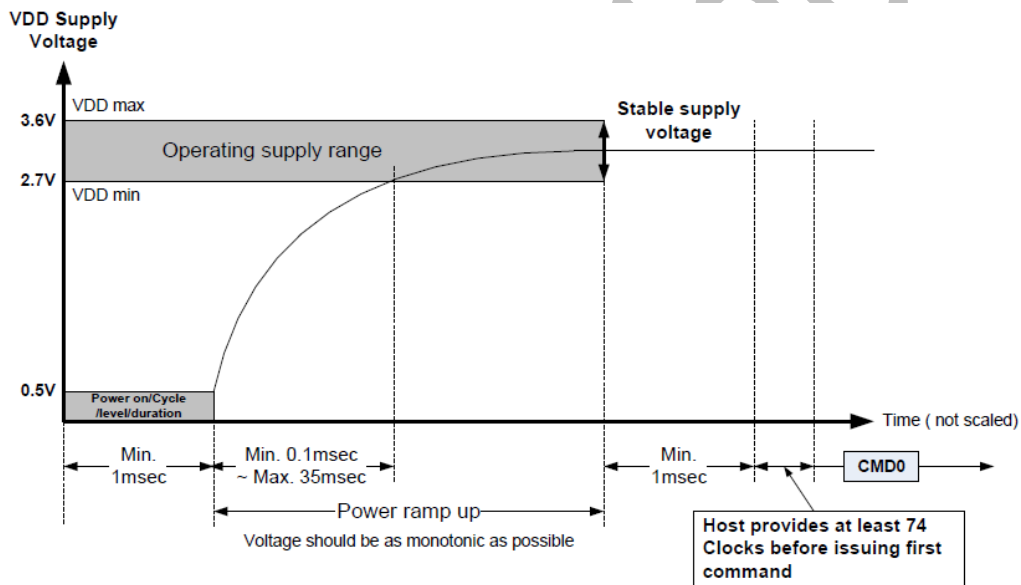
**Figure 4. Power-up Diagram**

- Power up time is defined as voltage rising time from 0 volt to VDD(min.) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

- Supply ramp up time provides the time that the power is built up to the operating level (the host supply voltage) and the time to wait until the SD card can accept the first command.
- The host shall supply power to the card so that the voltage is reached to VDD(min.) within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.
- After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.
- CMD8 is added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.
- ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

**6.4.2 Reset Level Power Up**

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



**Figure 5. change of Figure for power up**

- To assure a reliable SD Card hard reset of Power On and Power Cycle, Voltage level shall be below 0.5V and Time duration shall be at least 1ms.
- The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

- (1) Voltage of power ramp up should be monotonic as much as possible.
- (2) The minimum ramp up time should be 0.1ms.
- (3) The maximum ramp up time should be 35ms for 2.7~3.6V power supply

### 6.4.3 Power Down and Power Cycle

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5V for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5V for a minimum period of 1ms).

### 6.4.4 Bus Operating Conditions for 3.3V Signaling

- **Threshold Level for High Voltage Range**

Table 27. Threshold Level for High Voltage for I/O 3.3V

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V <sub>DD</sub>	2.7	3.6	V	
Output High Voltage	V <sub>OH</sub>	0.75* V <sub>DD</sub>		V	I <sub>OH</sub> =2mA V <sub>DD min</sub>
Output Low Voltage	V <sub>OL</sub>		0.125* V <sub>DD</sub>	V	I <sub>OL</sub> =2mA V <sub>DD min</sub>
Input High Voltage	V <sub>IH</sub>	0.625* V <sub>DD</sub>	V <sub>DD</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub>	V <sub>SS</sub> -0.3	0.25* V <sub>DD</sub>	V	
Power Up Time			250	ms	From 0V to V <sub>DD min</sub>

- **Peak Voltage and Leakage Current**

Table 28. Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V <sub>DD</sub> +0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

● **Bus Signal Line Load**

Table 29. Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R <sub>CMD</sub> R <sub>DAT</sub>	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line	C <sub>L</sub>		40	pF	1 card C <sub>HOST</sub> +C <sub>BUS</sub> shall not exceed 30pF
Card capacitance for each signal pin	C <sub>CARD</sub>		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card(pin1)	R <sub>DAT3</sub>	10	90	KΩ	May be used for card detection
Capacity Connected to Power Line	C <sub>C</sub>		5	uF	To prevent inrush current

● **Bus Signal Levels**

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

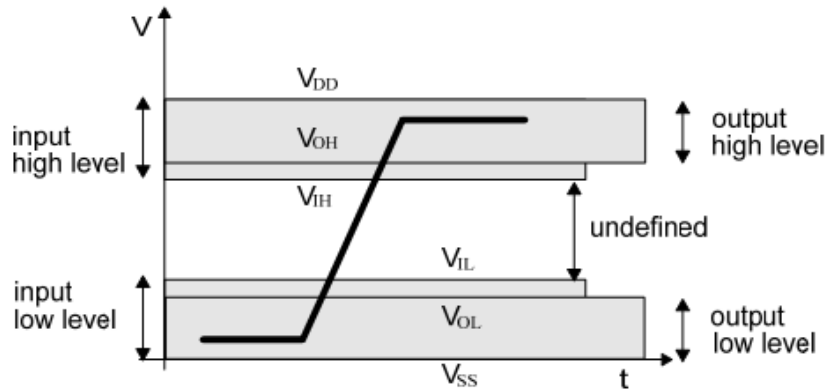


Figure 6. Bus Signal Levels for 3.3V Signaling

To meet the requirements of the the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specifide ranges shown in Table 6-2 for any VDD of the allowed voltage range:

● **Bus Timing(Default)**

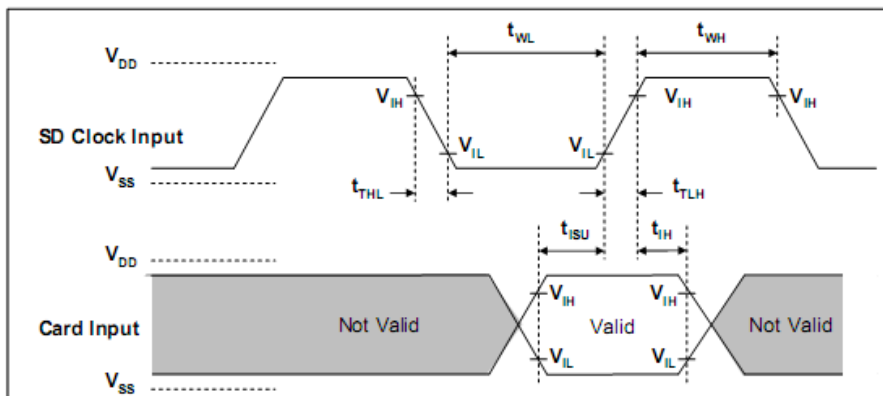


Figure 7. Card input Timing(Default Speed Card)

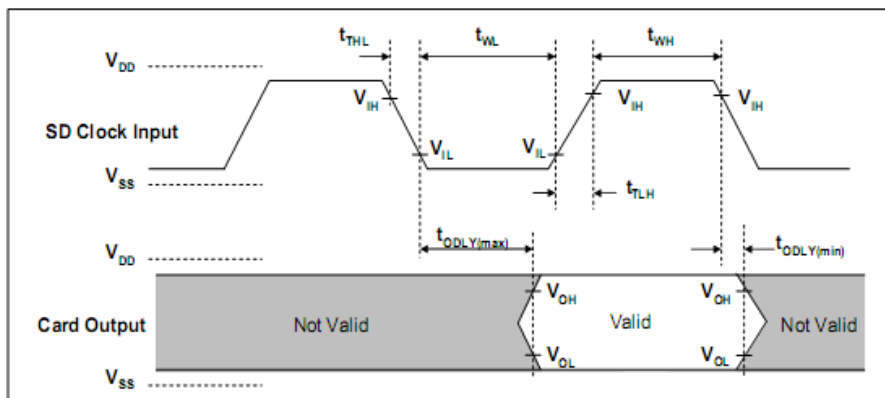


Figure 8. Card Output Timing(Default Speed Mode)

Table 30. Bus Timing-Parameters Values (Default Speed)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK (All values are referred to min (V <sub>IH</sub> ) and max (V <sub>IL</sub> ))					
Clock frequency data transfer Mode	f <sub>PP</sub>	0	25	MHz	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock frequency Identification Mode	f <sub>OD</sub>	0 <sup>1</sup> /100	400	KHz	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock low time	t <sub>WL</sub>	10		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock high time	t <sub>WH</sub>	10		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock rise time	t <sub>TLH</sub>		10	ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock fall time	t <sub>THL</sub>		10	ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	5		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Input hold time	t <sub>TH</sub>	5		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t <sub>ODLY</sub>	0	14	ns	C <sub>L</sub> ≤ 40pF (1 card)
Output Delay time during Identification Mode	t <sub>ODLY</sub>	0	50	ns	C <sub>L</sub> ≤ 40pF (1 card)

Note1:  
 0 Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required (refer to Chapter 4.4- Clock Control)

● Bus Timing(High-Speed Mode)

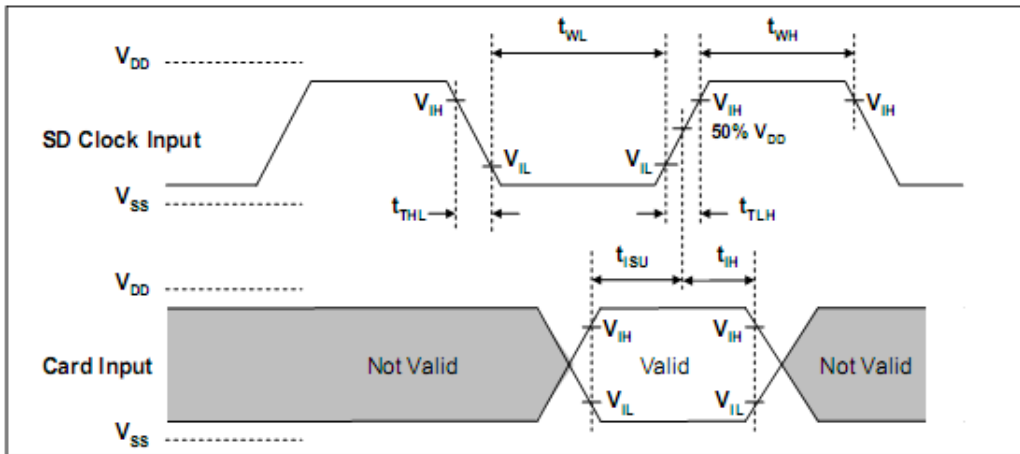


Figure 9. Card Input Timing(High Speed Card)

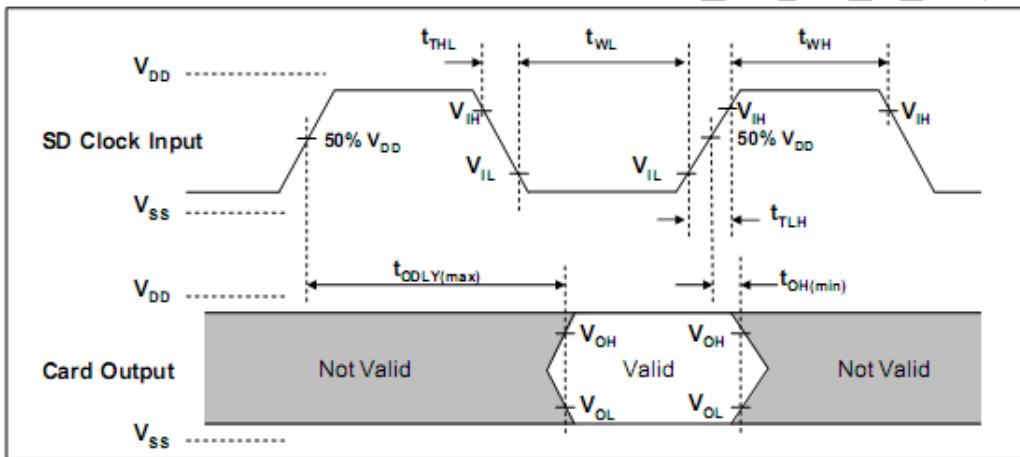


Figure 10. Card Output Timing(High Speed Mode)

Table 31. Bus Timing – Parameters Values(High Speed)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL))					
Clock frequency data transfer Mode	f <sub>PP</sub>	0	50	MHZ	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock low time	t <sub>WL</sub>	7		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock high time	t <sub>WH</sub>	7		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock rise time	t <sub>TLH</sub>		3	ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Clock fall time	t <sub>THL</sub>		3	ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	6		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Input hold time	t <sub>IH</sub>	2		ns	C <sub>CARD</sub> ≤ 10pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t <sub>ODLY</sub>		14	ns	C <sub>L</sub> ≤ 40pF (1 card)
Output Hold time	t <sub>OH</sub>	2.5		ns	C <sub>L</sub> ≥ 15pF (1 card)
Total System capacitance for each line	C <sub>L</sub>		40	pF	1 card

### 6.4.5 Driver Strength for 1.8V Signaling

- **Threshold Level for High Voltage Range**

**Table 32. Threshold Level for High Voltage For I/O 1.8V**

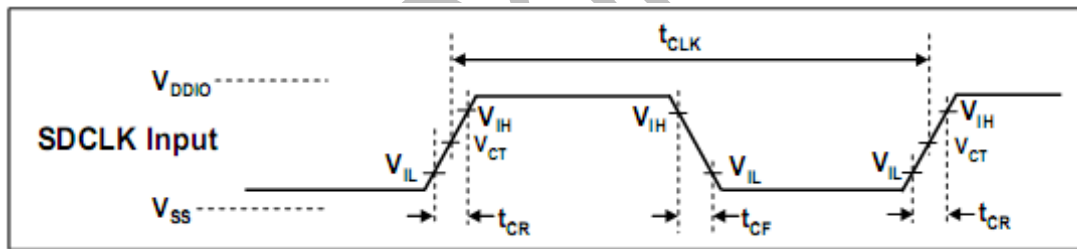
Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	$V_{DD}$	2.7	3.6	V	
Regulator Voltage	$V_{DDIO}$	1.7	1.95	V	Generated by $V_{DD}$
Output High Voltage	$V_{OH}$	1.4		V	$I_{OH}=2mA$ $V_{DD}$ min
Output Low Voltage	$V_{OL}$		0.45	V	$I_{OL}=2mA$ $V_{DD}$ min
Input High Voltage	$V_{IH}$	1.27	2.0	V	
Input Low Voltage	$V_{IL}$	$V_{SS}-0.3$	0.58	V	

- **Peak Voltage and Leakage Current**

**Table 33. Peak Voltage and Leakage Current**

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	$\mu A$	DAT3 pull-up is disconnected

- **Clock Timing**



**Figure 11. Clock Signal Timing**

**Table 34. Clock Signal Timing**

Symbol	Min	Max	Unit	Remark
$t_{CLK}$	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT}=0.975V$
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 0.96ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

● Card Input Timing

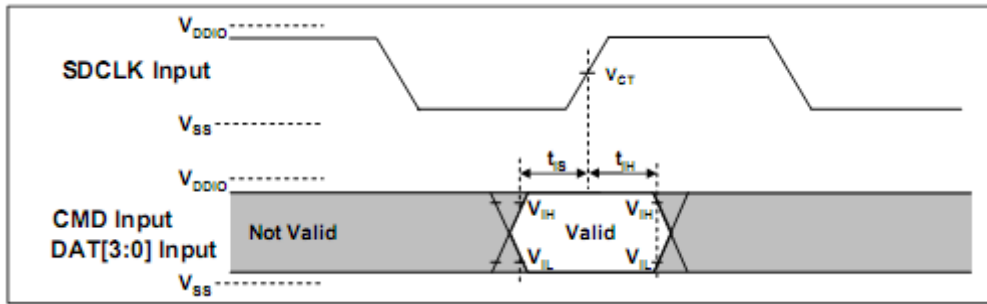


Figure 12. Card Input Timing

Table 35. SDR50 and SDR104 Input Timing

Symbol	Min	Max	Unit	SDR104 mode
$t_{IS}$	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

Symbol	Min	Max	Unit	SDR12, SDR25 and SDR50 modes
$t_{IS}$	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

● Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

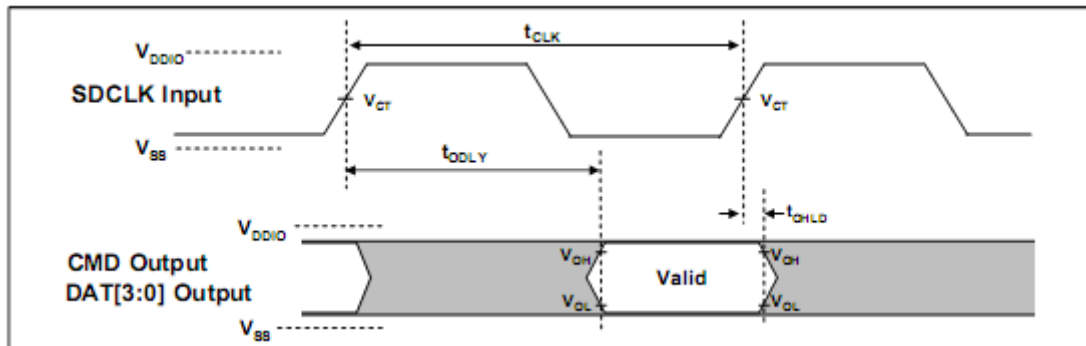


Figure 13. Output Timing of Fixed Data Window

Table 36. Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
$t_{ODLY}$	-	7.5	ns	$t_{CLK} \geq 10.0ns, C_L = 30pF$ , using driver Type B, for SDR50.
$t_{ODLY}$	-	14	ns	$t_{CLK} \geq 20.0ns, C_L = 40pF$ , using driver Type B, for SDR25 and SDR12.
$t_{OHLB}$	1.5	-	ns	Hold time at the $t_{ODLY}$ (min.). $C_L = 15pF$

● Output Timing of Variable Window (SDR104)

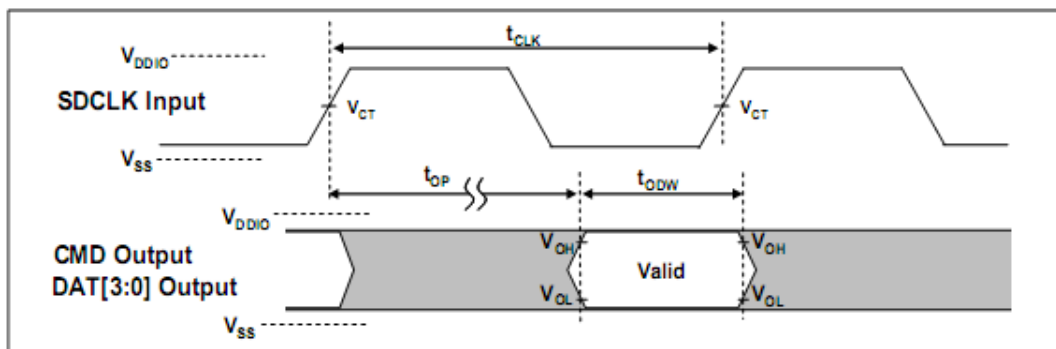


Figure 14. Output Timing of Variable Data Window for SDR104

Table 37. Output Timing of Variable Data Window

Symbol	Min	Max	Unit	Remark
$t_{OP}$	-	2	UI	Card Output Phase
$\Delta t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
$t_{ODW}$	0.60	-	UI	$t_{ODW} = 2.88ns$ at 208MHz

## 7 SD CARD FUNCTIONAL DESCRIPTION

### 7.1 General

FORESEE SD Card Functional Description contained in this chapter 4 of SDA Physical Layer Specification Version 6.1.

### 7.2 Card Identification Mode

While in Card Identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address(RCA). This operation is done to each card separately on its own CMD line. Refer to Section 4.2 of the SDA Physical Layer Specification, Version 6.1 for detail information and guide.

Note:

The products on this specification support UHS-I mode. For correct identification flow, please refer to Section 4.2 of the SDA Physical Layer Specification, Version 2.00.

### 7.3 Clock Control

The SD Memory Card bus clock signal can be used by the host to change the cards to energy saving mode or to control the data flow(to avoid under-run or over-run conditions) on the bus. Refer to Section 4.4 of the SDA Physical Layer Specification, Version 6.1 for detail information and guide.

## 7.4 Cyclic Redundancy Code

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block, per data line, is generated. The CRC is generated and checked as described in the Section 4.5 of the SDA Physical Layer Specification, Version 6.1.

## 7.5 Command

There are four kinds of commands defined to control the SD Card:

\* Broadcast commands (bc), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated then each card will accept it separately on his turn.

\* Broadcast commands with response (bcr) - response from all cards simultaneously. Since there is no Open Drain mode in SD Card, this type of command is used only if all the CMD lines are separated. The command will be accepted and responded to by every card separately.

\* Addressed (point-to-point) commands (ac) - no data transfer on DAT lines

\* Addressed (point-to-point) data transfer commands (adtc), data transfer on DAT lines

All commands and responses are sent over the CMD line of the SD Card bus. The command transmission always starts with the left bit of the bit string corresponding to the command code word. For more details, refer to the Section 4.7 of the SDA Physical Layer Specification, Version 6.1.

Note:

Limited Vendor CMD information, only for certain customer and application, can be provided under appropriate purpose of usage.

## 7.6 Memory Array Partitioning

The basic unit of data transfer to/from the SD Card is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

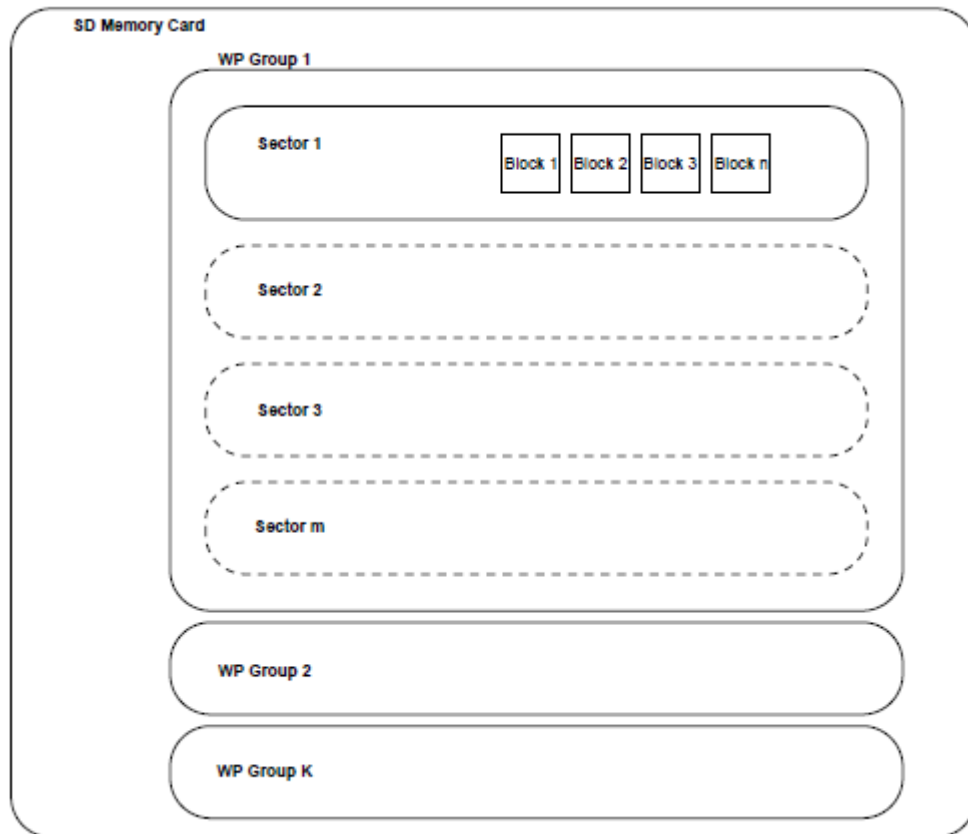


Figure 15. Write Protection Hierarchy

For block oriented commands, the following definition is used:

- **Block:** is the unit that is related to the block oriented read and write commands. Its size is the number of bytes that will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.
- For devices that have erasable memory cells, special erase commands are defined. The granularity of the erasable units is in general not the same as for the block oriented commands:
- **Sector:** is the unit that is related to the erase commands. Its size is the number of blocks that will be erased in one portion. The size of a sector is fixed for each device. The information about the sector size (in blocks) is stored in the CSD. Note: that if the card specifies AU size, sector size should be ignored.
- **AU (Allocation Unit):** is a physical boundary of the card and consists of one or more blocks and its size depends on each card. The maximum AU size is defined for memory capacity. Furthermore AU is the minimal unit in which the card guarantees its performance for devices which complies with Speed Class Specification. The information about the size and the Speed Class are stored in the SD Status. AU is also used to calculate the erase timeout and UHS speed Grade
- **WP-Group:** is the minimal unit that may have individual write protection for devices which support write-protected group. Its size is the number of groups that will be write-protected by one bit. The size of a WP-group is fixed for each device. The information about the size is stored in the CSD. The High Capacity SD Memory Card does not support the write protect group command.

## 7.7 Timings

Refer to Section 4.12 of the SDA Physical Layer Specification, Version 6.1 for detail information and guide<sup>1</sup>

Note1:

The product on this specification supports UHS-I mode.

## 7.8 Speed Class Specification

Refer to Section 4.13 of the SDA Physical Layer Specification, Version 6.1 for detail information and guide<sup>1</sup>

Note1:

The product on this specification supports UHS-I mode.

## 7.9 Erase Timeout Calculation

Refer to Section 4.14 of the SDA Physical Layer Specification, Version 6.1 for detail information and guide<sup>1</sup>

Note1:

The product on this specification supports UHS-I mode

## 8 Mechanical Specification

This section describes the mechanical and electrical features, as well as SEC SD Card environmental reliability and durability specifications. For more details you can refer to SDA Physical Layer Specification Version 2.00, Section 8.1. For more details and Section 3.0 Mechanical Specification for SD Memory Card.



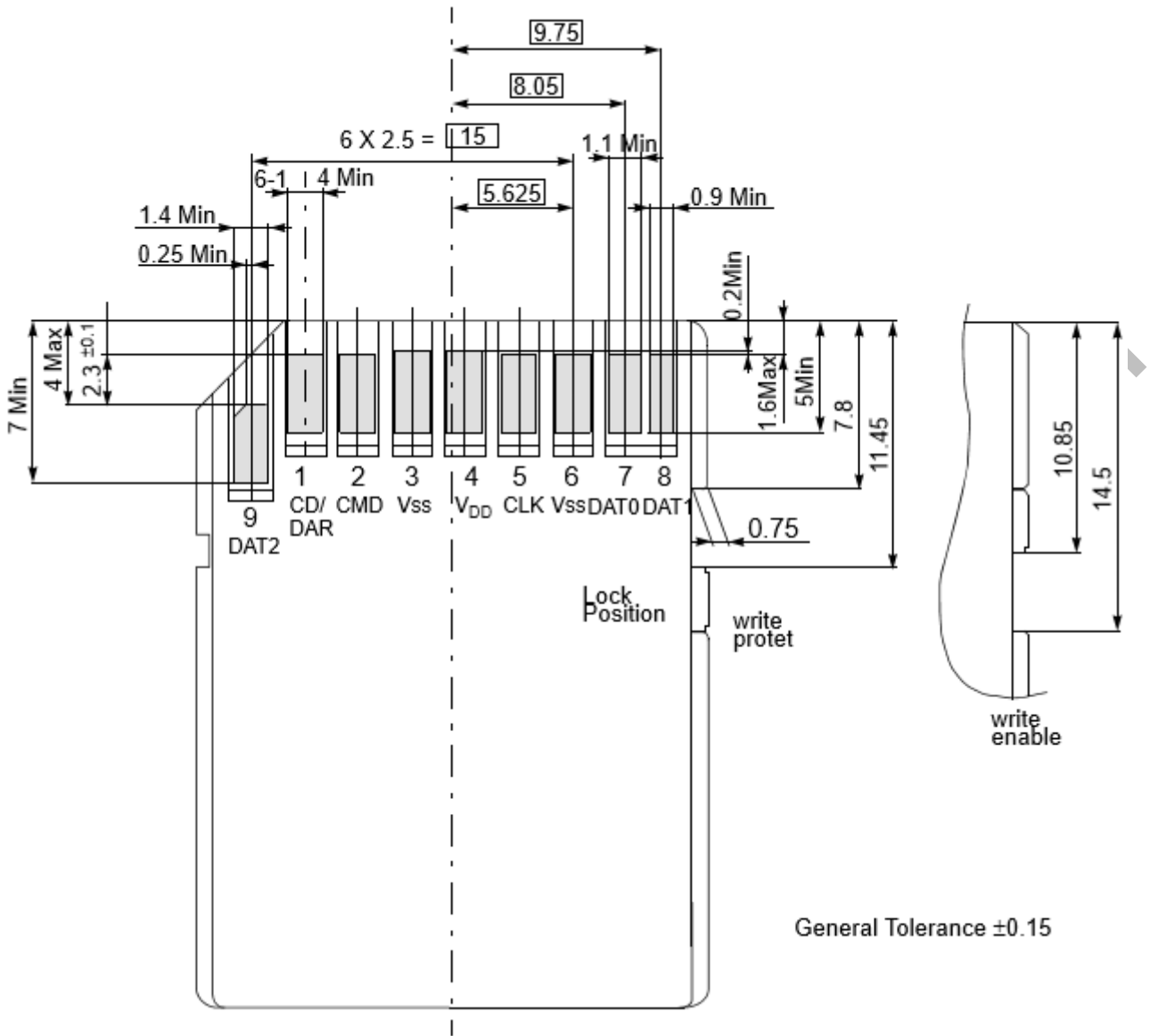


Figure 17. Mechanical Description: Bottom View

## 9 Marking



Figure 18. Marking