FORESEE DDR4 SDRAM UDIMM

Lead-Free & Halogen-Free
(RoHS Compliant)

Datasheet

Version: 1.1

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Revision History

Revision NO.	History	Draft Date	Remark
1.0	First SPEC. Release	Jun. 2021	-
1.1	Modify part of the description	Jul. 2021	-

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1. Description

FORESEE Unbuffered DDR4 SDRAM DIMMs (Unbuffered Double Data Rate Syn-chronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

2. Features

- VDD = 1.2V ± 60mv
- VPP = 2.5V (2.375V~2.75V)
- 8-bit pre-fetch
- On Die Termination using ODT pin
- Data Bus inversion (DBI) for data bus
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- CapabilityPPR and sPPR is supported
- All of Lead-Free products are compliant for RoHS
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

3. Ordering Information

Part Number	Density	Speed	Component Composition	# of ranks
FD4AU2666C4GCQ	4GB	DDR4-2666	512Mx16*4	1
FD4AU2666C8GCQ	8GB	DDR4-2666	1Gx8*8	1

4. Key Parameters

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
2666V	2666	0.75	19	14.25	14.25	32	46.75	19-19-19

5. Address Table

Organization	Number of bank Groups	Bank group Address	Bank Address	Row Address	Column Address
512Mx16	2	BG0	BA[1:0]	A[15:0]	A[9:0]
1Gx8	4	BG[1:0]	BA[1:0]	A[15:0]	A[9:0]

X XX X X XXXX X XX X X

Module Manufacturer
F=FORESEE

DRAM Technology
D3=DDR3
D4=DDR4
D5=DDR5

Voltage
A=1.2V
B=1.35V
C=1.5V
D=1.1V

Product Family
U=UDIMM
S=SODIMM
E=ECC DIMM
R=RDIMM

Speed
1600=1600Mbps
1866=1866Mbps
2133=2133Mbps
2400=2400Mbps
2666=2666Mbps
2933=2933Mbps
3200=3200Mbps
⋮

Operating Temperatures
C=0~85℃
I=-25~85℃
W=-40~85℃

Density
4G=4GB
8G=8GB
QG=16GB
WG=32GB

DRAM Manufacturer
C=CXMT
M=Micron
S=Samsung
T/Z=Longsys

Die Revision

6. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17	SDRAM address bus	CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
BA0,BA1	SDRAM bank select	SCL	I2C serial bus clock for SPD-TSE
BG0, BG1	SDRAM bank group select	SDA	I2C serial bus data line for SPD-TSE
RAS_n	SDRAM row address strobe	SA0–SA2	I2C slave address select for SPD-TSE
CAS_n	SDRAM column address strobe	PARITY	SDRAM parity input
WE_n	SDRAM write enable	VDD	SDRAM I/O and core power supply
CS0_n, CS1_n	DIMM Rank Select Lines	12 V	Optional power Supply on socket but not used on UDIMM
CKE0, CKE1	SDRAM clock enable lines	VREFCA	
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t- TDQS8_t TDQS0_c- TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs	RESET_n	Set DRAMs to a Known State
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	VTT	SDRAM I/O termination supply
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x64 DIMMs)	RFU	Reserved for future use
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)		

Note:

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

7. Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE(CKE1)	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE are disabled during Self-Refresh.
CS_n,(CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM.When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.

Symbol	Type	Function
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t,DQS_c, DQSU_t,DQSU_c, DQSL_t, DQSL_c	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t , DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.

Symbol	Type	Function
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin works as input.Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V ± 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration.

Note:

1. Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

8. Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	12V	145	12V	37	VSS	181	DQ29
2	VSS	146	VREFCA	38	DQ24	182	VSS
3	DQ4	147	VSS	39	VSS	183	DQ25
4	VSS	148	DQ5	40	DM3_n,DBI3_n DQS12_t,TDQS12_t	184	VSS
5	DQ0	149	VSS	41	DQS12_c,TDQS12_c	185	DQS3_c
6	VSS	150	DQ1	42	VSS	186	DQS3_t
7	DM0_n,DBI_n DQS9_t,TDQS9_t	151	VSS	43	DQ30	187	VSS
8	DQS9_c,TDQS9_c	152	DQS0_c	44	VSS	188	DQ31
9	VSS	153	DQS0_t	45	DQ26	189	VSS
10	DQ6	154	VSS	46	VSS	190	DQ27
11	VSS	155	DQ7	47	CB4,NC	191	VSS
12	DQ2	156	VSS	48	VSS	192	CB5,NC
13	VSS	157	DQ3	49	CB0,NC	193	VSS
14	DQ12	158	VSS	50	VSS	194	CB1,NC
15	VSS	159	DQ13	51	DM8_n,DBI_n DQS17_t,TDQS17_t	195	VSS
16	DQ8	160	VSS	52	DQS17_c,TDQS17_c	196	DQS8_c
17	VSS	161	DQ9	53	VSS	197	DQS8_t
18	DM1_n,DBI1_n DQS10_t,TDQS10_t	162	VSS	54	CB6,NC	198	VSS
19	DQS10_c,TDQS10_c	163	DQS1_c	55	VSS	199	CB7,NC
20	VSS	164	DQS1_t	56	CB2,NC	200	VSS
21	DQ14	165	VSS	57	VSS	201	CB3,NC
22	VSS	166	DQ15	58	RESET_n	202	VSS
23	DQ10	167	VSS	59	VDD	203	CKE1
24	VSS	168	DQ11	60	ACT_n	204	VDD
25	DQ20	169	VSS	61	VDD	205	RFU
26	VSS	170	DQ21	62	ACT_n	206	VDD
27	DQ16	171	VSS	63	BG0	207	BG1
28	VSS	172	DQ17	64	VDD	208	ALERT_n
29	DM2_n,DBI2_n DQS11_t,TDQS11_t	173	VSS	65	A12	209	VDD
30	DQS11_c,TDQS11_c	174	DQS2_c	66	A9	210	A11
31	VSS	175	DQS2_t	67	VDD	211	A7
32	DQ22	176	VSS	68	A8	212	VDD
33	VSS	177	DQ23	69	A6	213	A5
34	DQ18	178	VSS	70	VDD	214	A4
35	VSS	179	DQ19	71	A3	215	VDD
36	DQ28	180	VSS	72	A1	216	A2

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
73	VDD	217	VDD	108	DQ40	252	VSS
74	CK0_t	218	CK1_t	109	VSS	253	DQ41
75	CK0_c	219	CK1_c	110	DM5_n,DBI5_n DQS14_t,TDQS14_t	254	VSS
76	VDD	220	VDD	111	DQS14_c,TDQS14_c	255	DQS5_c
77	VTT	221	VTT	112	VSS	256	DQS3_t
KEY				113	DQ46	257	VSS
78	EVENT_n	222	PARITY	114	VSS	258	DQ47
79	A0	223	VDD	115	DQ42	259	VSS
80	VDD	224	BA1	116	VSS	260	DQ43
81	BA0	225	A10/AP	117	DQ52	261	VSS
82	RAS_n/A16	226	VDD	118	VSS	262	DQ53
83	VDD	227	RFU	119	DQ48	263	VSS
84	CS0_n	228	WE_n/A14	120	VSS	264	DQ49
85	VDD	229	VDD	121	DM6_n,DBI6_n DQS15_t,TDQS15_t	265	VSS
86	CAS_n/A15	230	NC	122	DQS15_c,TDQS15_c	266	DQS6_c
87	ODT0	231	VDD	123	VSS	267	DQS6_t
88	VDD	232	A13	124	DQ54	268	VSS
89	CS1_n	233	VDD	125	VSS	269	DQ55
90	VDD	234	NC	126	DQ50	270	VSS
91	ODT1	235	NC	127	VSS	271	DQ51
92	VDD	236	VDD	128	DQ60	272	VSS
93	S2_n,C[0]	237	NC,CS3_n,C1	129	VSS	273	DQ61
94	VSS	238	SA2	130	DQ56	274	VSS
95	DQ36	239	VSS	131	VSS	275	DQ57
96	VSS	240	DQ37	132	DM7_n,DBI7_n DQS16_t,TDQS16_t	276	VSS
97	DQ32	241	VSS	133	DQS16_c,TDQS16_c	277	DQS7_c
98	VSS	242	DQ33	134	VSS	278	DQS7_t
99	DM4_n,DBI4_n DQS13_t,TDQS13_t	243	VSS	135	DQ62	279	VSS
100	DQS13_c,TDQS13_c	244	DQS4_c	136	VSS	280	DQ63
101	VSS	245	DQS4_t	137	DQ58	281	VSS
102	DQ38	246	VSS	138	VSS	282	DQ59
103	VSS	247	DQ39	139	SA0	283	VSS
104	DQ34	248	VSS	140	SA1	284	VDDSPD
105	VSS	249	DQ35	141	SCL	285	SDA
106	DQ44	250	VSS	142	VPP	286	VPP
107	VSS	251	DQ45	143	VPP	287	VPP
				144	RFU	288	VPP

9. DQ Map

Description: DDRIV SDRAM, Single-Rank, x8-FBGA 78-Ball-based, x64 Unbuffered, 288-pin UDIMM

Module Pin Number	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin Number	Module DQ	Damping RES.	IC No.	IC DQ
5	0	RN1(2-3)	U1	3	16	8	RN7(2-3)	U2	3
150	1	RN3(1-4)		1	161	9	RN5(1-4)		1
12	2	RN2(2-3)		2	23	10	RN8(2-3)		2
157	3	RN4(1-4)		0	168	11	RN6(1-4)		0
3	4	RN1(1-4)		7	14	12	RN7(1-4)		7
148	5	RN3(2-3)		5	159	13	RN5(2-3)		5
10	6	RN2(1-4)		6	21	14	RN8(1-4)		6
155	7	RN4(2-3)		4	166	15	RN6(2-3)		4
27	16	RN9(2-3)	U3	3	38	24	RN15(2-3)	U5	3
172	17	RN11(1-4)		1	183	25	RN13(1-4)		1
34	18	RN12(2-3)		2	45	26	RN14(2-3)		2
179	19	RN10(1-4)		0	190	27	RN16(1-4)		0
25	20	RN9(1-4)		7	36	28	RN15(1-4)		7
170	21	RN11(2-3)		5	181	29	RN13(2-3)		5
32	22	RN12(1-4)		6	43	30	RN14(1-4)		6
177	23	RN10(2-3)		4	188	31	RN16(2-3)		4
97	32	RN17(2-3)	U5	3	108	40	RN21(2-3)	U6	3
242	33	RN19(1-4)		1	253	41	RN23(1-4)		1
104	34	RN20(2-3)		2	115	42	RN24(2-3)		2
249	35	RN18(1-4)		0	260	43	RN22(1-4)		0
95	36	RN17(1-4)		7	106	44	RN21(1-4)		7
240	37	RN19(2-3)		5	251	45	RN23(2-3)		5
102	38	RN20(1-4)		6	113	46	RN24(1-4)		6
247	39	RN18(2-3)		4	258	47	RN22(2-3)		4
119	48	RN26(2-3)	U7	3	130	56	RN28(2-3)	U8	3
264	49	RN25(1-4)		1	275	57	RN30(1-4)		1
126	50	RN45(2-3)		2	137	58	RN29(2-3)		2
271	51	RN27(1-4)		0	282	59	RN31(1-4)		0
117	52	RN26(1-4)		7	128	60	RN28(1-4)		7
262	53	RN25(2-3)		5	273	61	RN30(2-3)		5
124	54	RN45(1-4)		6	135	62	RN29(1-4)		6
269	55	RN27(2-3)		4	280	63	RN31(2-3)		4

First check the SPD data and EEPROM. Then check the following components for other problem.

	Clock loading	Boot failure
1-RANK	R24,RN47	SPD data U19

Description: DDRIV SDRAM, Single-Rank, x16-FBGA 96-Ball-based, x64 UNBUFFERED, 288-pin DIMM

Module Pin Number	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin Number	Module DQ	Damping RES.	IC No.	IC DQ
5	0	RN9(3-6)	U1	3	27	16	RN15(3-6)	U2	3
150	1	RN9(4-5)		1	172	17	RN15(4-5)		1
12	2	RN11(3-6)		2	34	18	RN17(3-6)		2
157	3	RN11(4-5)		0	179	19	RN17(4-5)		0
3	4	RN9(1-8)		7	25	20	RN15(1-8)		7
148	5	RN9(2-7)		5	170	21	RN15(2-7)		5
10	6	RN11(1-8)		6	32	22	RN17(1-8)		6
155	7	RN11(2-7)		4	177	23	RN17(2-7)		4
16	8	RN12(3-6)		9	38	24	RN18(3-6)		9
161	9	RN12(4-5)		11	183	25	RN18(4-5)		11
23	10	RN14(3-6)		10	45	26	RN20(3-6)		10
168	11	RN14(4-5)		8	190	27	RN20(4-5)		8
14	12	RN12(1-8)		15	36	28	RN18(1-8)		15
159	13	RN12(2-7)		13	181	29	RN18(2-7)		13
21	14	RN14(1-8)		12	43	30	RN20(1-8)		12
166	15	RN14(2-7)		14	188	31	RN20(2-7)		14
97	32	RN21(3-6)	U4	3	119	48	RN27(3-6)	U5	3
242	33	RN21(4-5)		1	264	49	RN27(4-5)		1
104	34	RN23(3-6)		2	126	50	RN29(3-6)		2
249	35	RN23(4-5)		0	271	51	RN29(4-5)		0
95	36	RN21(1-8)		7	117	52	RN27(1-8)		7
240	37	RN21(2-7)		5	262	53	RN27(2-7)		5
102	38	RN23(1-8)		6	124	54	RN29(1-8)		6
247	39	RN23(2-7)		4	269	55	RN29(2-7)		4
108	40	RN24(3-6)		9	130	56	RN30(3-6)		9
253	41	RN24(4-5)		11	275	57	RN30(4-5)		11
115	42	RN26(3-6)		10	137	58	RN32(3-6)		10
260	43	RN26(4-5)		8	282	59	RN32(4-5)		8
106	44	RN24(1-8)		15	128	60	RN30(1-8)		15
251	45	RN24(2-7)		13	273	61	RN30(2-7)		13
113	46	RN26(1-8)		12	135	62	RN32(1-8)		12
258	47	RN26(2-7)		14	280	63	RN32(2-7)		14

First check the SPD data and EEPROM. Then check the following components for other problem.

	Clock loading	Boot failure
1-RANK	R7,RN8	SPD data U3

10. Speed Bins

DDR4-2666 Speed Bins and Operations

Speed Bin		DDR4-2666V		Unit
CL-nRCD-nRP		19-19-19		
Parameter	Symbol	ns	max	
Internal READ command to first data	tAA	14.25	18.00	ns
Internal READ command to first data with read DBI enabled	tAA_DBI	tAA(Min) + 3nCK	tAA(Max) + 3nCK	ns
ACT to internal READ or WRITE delay time	tRCD	14.25	-	ns
PRE command period	tRP	14.25	-	ns
ACT to PRE command Period	tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period	tRC	46.25	-	ns

11. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

12. Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V
V_{IN}, V_{OUT}	Voltage on any relative to VSS	-0.3 ~ 1.5	V
V_{STG}	Storage Temperature	-55 to +100	℃

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

13. AC & DC Operating Conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.14	1.2	VDD	V
VDDQ	Supply Voltage for Output	1.14	1.2	VDDQ	V
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

14. Functional Diagram

Figure 1: FD4AU2666C8GCQ

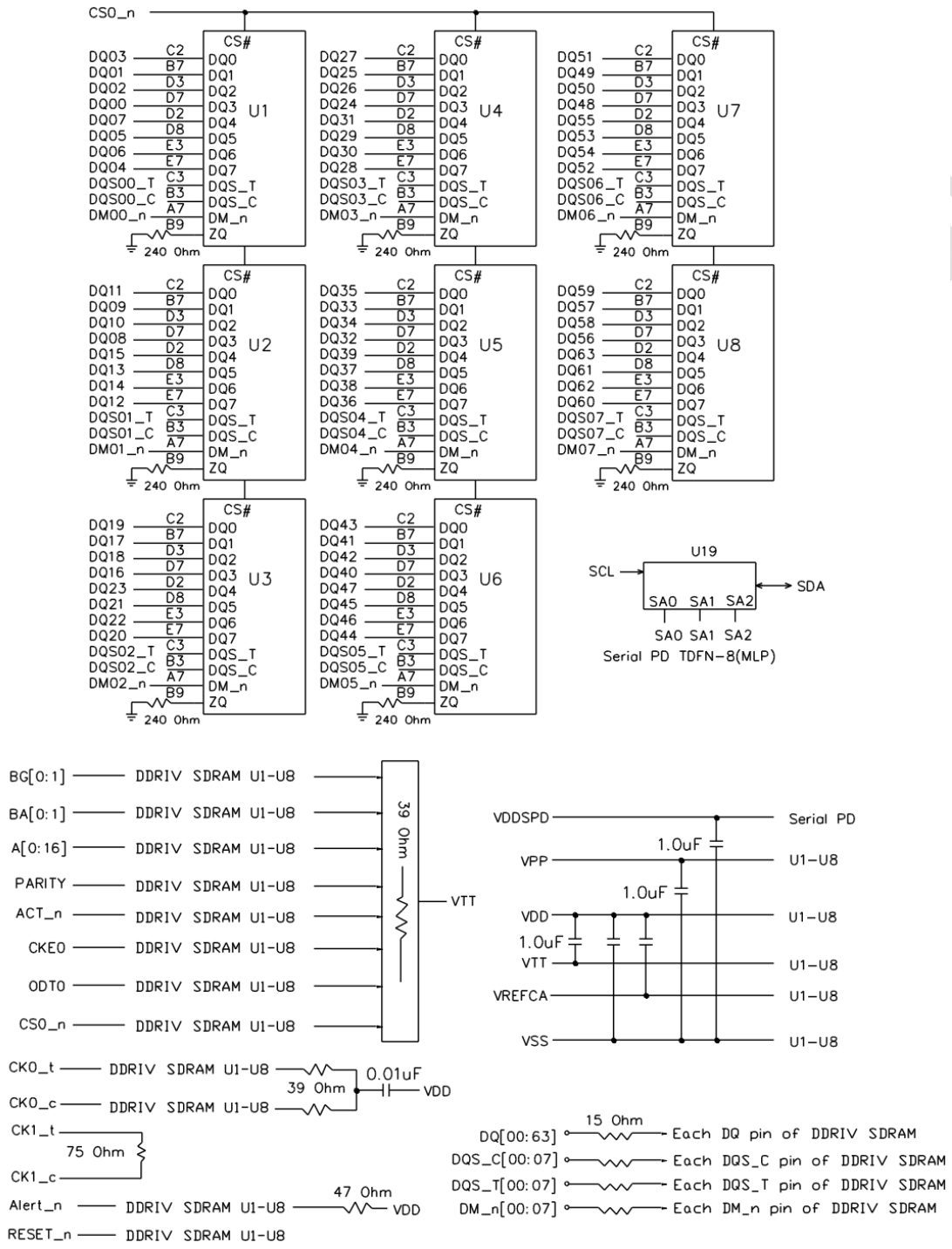
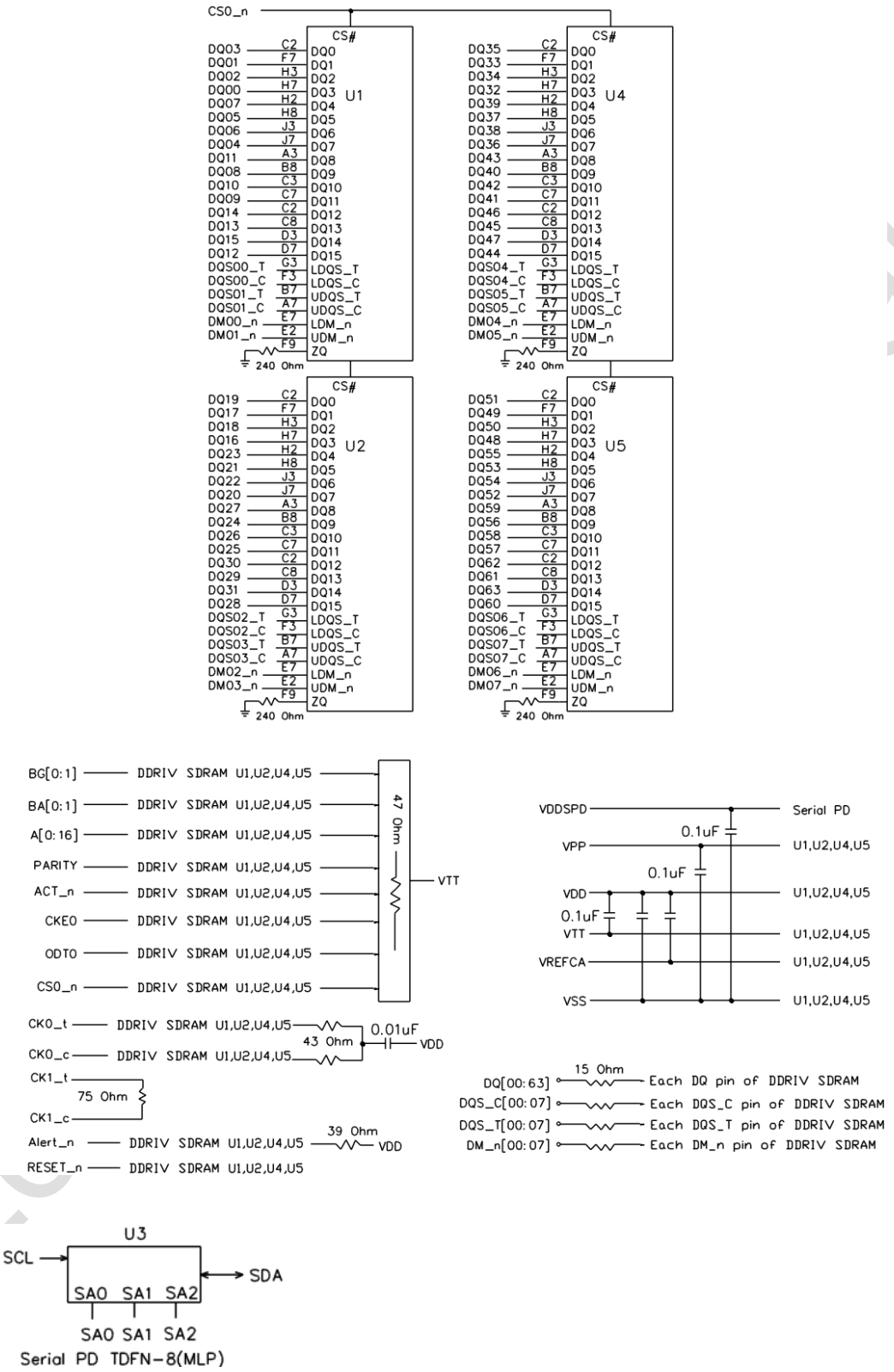


Figure 2: FD4AU2666C4GCQ



15. PCB Specifications

General

1. Board size: 133.35 x 31.25 mm ± 0.15 mm

2. Thickness: 1.4 ± 0.1 mm

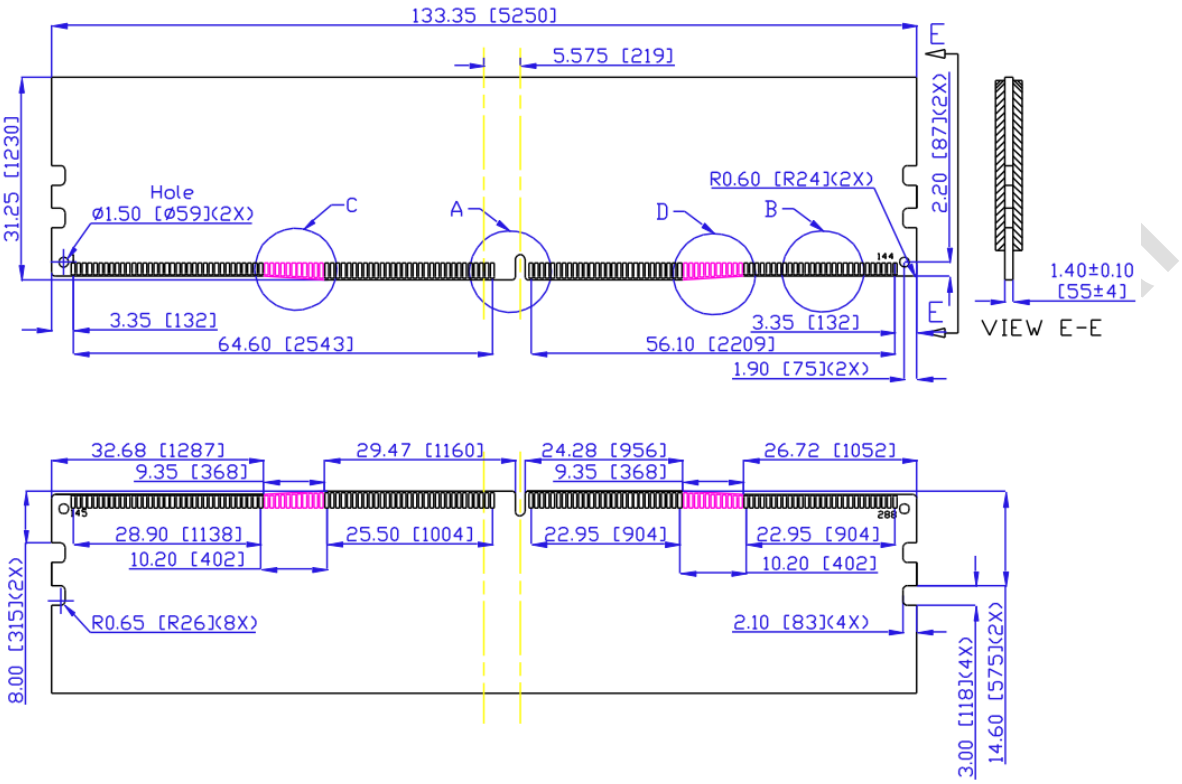
3. Pin count: 288 PIN

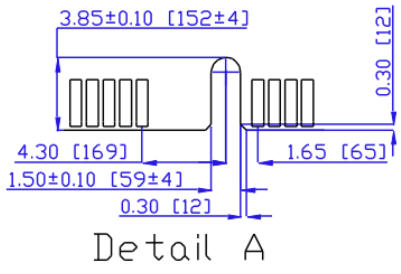
PCB Material

1. RoHS

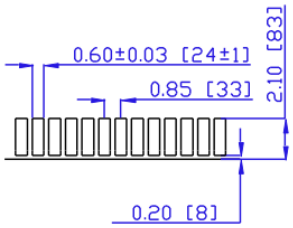
2. Glass Epoxy FR4, .UL 94V-0

16. Module Dimensions

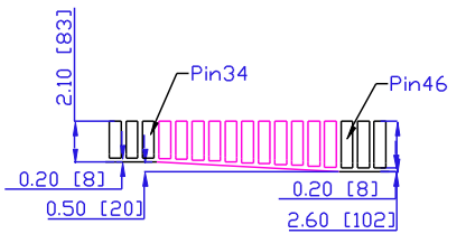




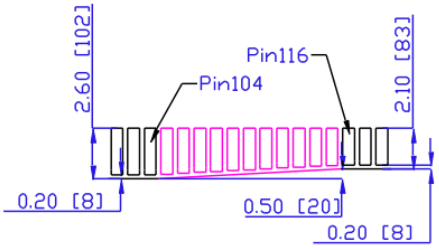
Detail A



Detail B



Detail C



Detail D

Units: millimeters