FORESEE 8GB DDR4 2666
SO-DIMM Datasheet

Version: 1.0

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Revision History

Revision No.	History	Draft Date	Remark
1.0	Release	Jan 2020	

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1. Description

FORESEE Unbuffered Small Outline DDR4 SDRAM DIMMs (Unbuffered Small Outine Double Data Rate Syn-chronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered Small Outline DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

2. Features

- VDD = VDDQ = 1.2V ± 60mV
- 16 Banks (4 Bank Groups)
- 8-bit pre-fetch
- On Die Termination using ODT pin
- (Data Bus Inversion)
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- capabilityPPR and sPPR is supported
- All of Lead-Free products are compliant for RoHS

3. Ordering Information

Part Number	Density	Speed	Component Composition	# of ranks
FD4AS2666C8GSC	8GB	DDR4 2666	1Gx8*8	1

4. Key Parameters

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
2666V	2666	0.750	19	14.25	14.25	32	46.25	19-19-19

5. Address Table

	1G*8
of Bank Groups	4
Bank group Address	BG0~BG1
Bank Address in a BG	BA0~BA1
Row Address	A0~A15
Column Address	A0~A9
Page size	1 KB

F D4 A S 2666 C 8G S C

F=FORESEE

DDR3=D3
DDR4=D4
DDR5=D5

A=1.2V
B=1.35V
C=1.5V

U=UDIMM
S=SO-DIMM
E=ECC DIMM
R=Register DIMM
⋮

1600=1600Mbps
2400=2400Mbps
2666=2666Mbps
2933=2933Mbps
3200=3200Mbps
⋮

4G=4GB
8G=8GB
QG=16GB
WG=32GB

C= 0-85℃
I =-25-85℃
W=-40-85℃

S=SAMSUNG

C=SAMSUNG C DIE

6. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃	1,2,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

7. Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
VIN, VOUT	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
3. VPP must be equal or greater than VDD/VDDQ at all times.

8. AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

9. x8 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n /TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	TEN	G
H	VDD	WE_n/A14	ACT_n				CAS_n/A15	RAS_n	VSS	H
J	VREFCA	BG0	A10/AP				A12/BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

10. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD/TS
RAS_n1	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n2	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n3	SDRAM write enable	VPP	SDRAM activating power supply
CSx_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)	VTT	mination supply for the Address, Com- mand and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Notes:

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.
4. The is a generic definition.

11. Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c,ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 conurations. For x16 conuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

Symbol	Type	Function
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 conuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD},

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.

Symbol	Type	Function
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note:

1. Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

12. Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VSS	2	VSS	131	A3	132	A2
3	DQ5	4	DQ4	133	A1	134	EVENT_n
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ1	8	DQ0	137	CK0_t	138	CK1_t
9	VSS	10	VSS	139	CK0_c	140	CK1_C
11	DQS0_C	12	DM0_n, DBI0_n	141	VDD	142	VDD
13	DQS0_t	14	VSS	143	PARITY	144	A0
15	VSS	16	DQ6	KEY			
17	DQ7	18	VSS				
19	VSS	20	DQ2	145	BA1	146	A10/AP
21	DQ3	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	A14/WE_n	152	A16/RAS_n
27	VSS	28	DQ8	153	VDD	154	VDD
29	DQ9	30	VSS	155	ODT0	156	A15/CAS_n
31	VSS	32	DQS1_C	157	CS1_n	158	A13
33	DM1_n, DBI1_n	34	DQS1_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	C0, CS2_n, NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	C1, CS3_n, NC	166	SA2
41	DQ10	42	DQ11	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS
51	VSS	52	VSS	177	DQS4_C	178	DM4_n, DBI4_n
53	DQS2_c	54	DM2_n, DBI2_n	179	DQS4_t	180	VSS
55	DQS2_t	56	VSS	181	VSS	182	DQ39
57	VSS	58	DQ22	183	DQ38	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ45
65	VSS	66	DQ28	191	DQ44	192	VSS
67	DQ29	68	VSS	193	VSS	194	DQ41
69	VSS	70	DQ24	195	DQ40	196	VSS
71	DQ25	72	VSS	197	VSS	198	DQS5_c

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
73	VSS	74	DQS3_c	199	DM5_n, DBI5_n	200	DQS5_t
75	DM3_n, DBI3_n	76	DQS3_t	201	VSS	202	VSS
77	VSS	78	VSS	203	DQ46	204	DQ47
79	DQ30	80	DQ31	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ26	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5, NC	88	CB4, NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1, NC	92	CB0, NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQS6_C	220	DM6_n, DBI6_n
95	DQS8_c	96	DBI8_n	221	DQS6_t	222	VSS
97	DQS8_t	98	VSS	223	VSS	224	DQ54
99	VSS	100	CB6, NC	225	DQ55	226	VSS
101	CB2, NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7, NC	229	DQ51	230	VSS
105	CB3, NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	DQ61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ56	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQS7_c
115	BG0	116	ALERT_n	241	DM7_n, DBI7_n	242	DQS7_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	DQ62	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	DQ58	250	DQ59
125	A8	126	A5	251	VSS	252	VSS
127	A6	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSPD	256	SA0
				257	VPP	258	VTT
				259	VPP	260	SA1

13. DDR4-2666 Speed Bins and Operations

Speed Bin		DDR4-2666V		Unit	NOTE
CL-nRCD-nRP		19-19-19		ns	11
Parameter	Symbol	min	max	ns	11
Internal READ command to first data	tAA	14.25[14] (13.75)[5,12]	18.00	ns	11
Internal READ command to first data with read DBI enabled	tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal READ or WRITE delay time	tRCD	14.25 (13.75)[5,12]	-	ns	11
PRE command period	tRP	14.25 (13.75)[5,12]	-	ns	11
ACT to PRE command Period	tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period	tRC	46.25 (45.75)[5,12]	-	ns	11

14. Trouble shooting Guide

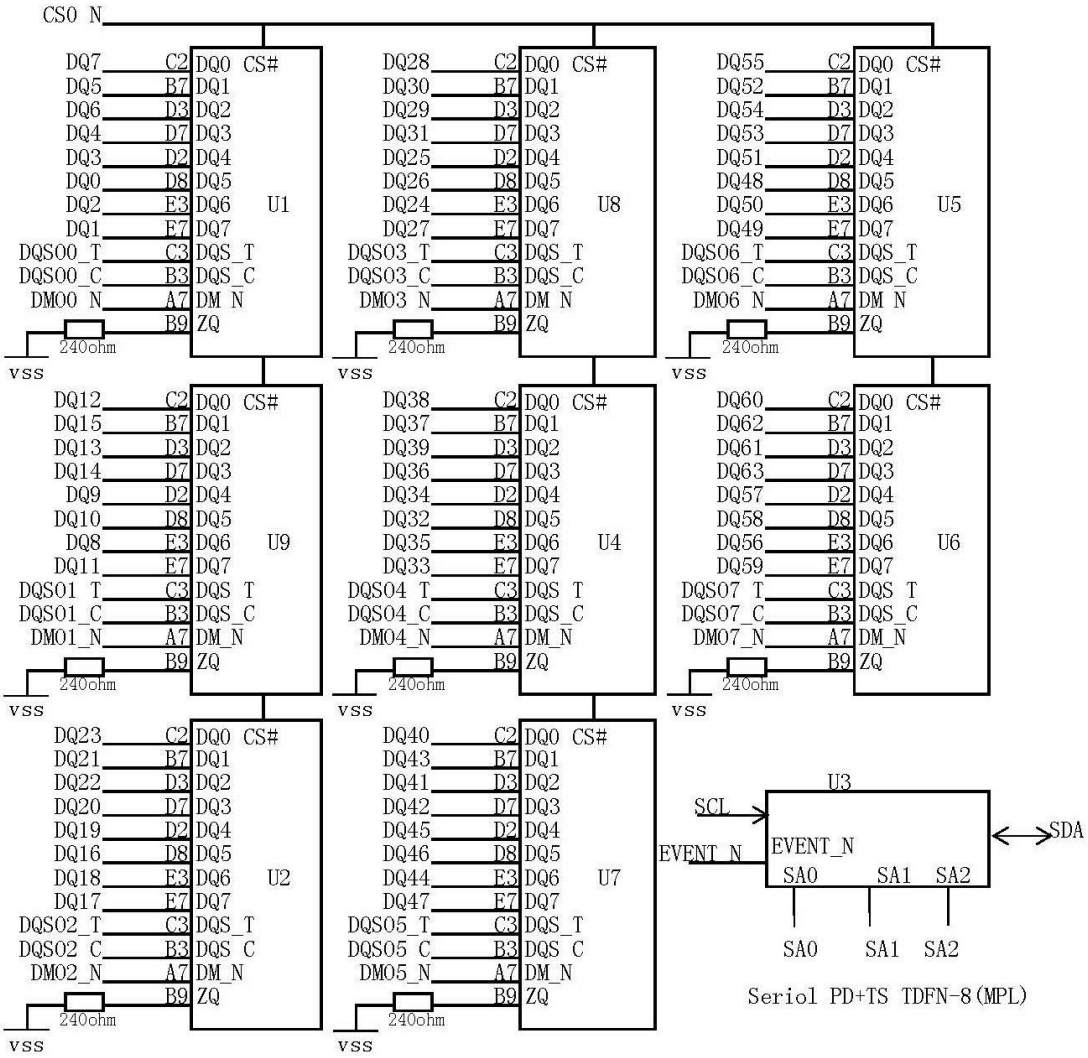
Description: DDRIV SDRAM, Single-Rank, x8-FBGA 78-Ball-based, x64 Unbuffered, 260-pin SO DIMM

Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ
8	0	R98	U1	5	28	8	R93	U9	6
7	1	R6		7	29	9	R12		4
20	2	R95		6	41	10	R15		5
21	3	R10		4	42	11	R89		7
4	4	R199		3	24	12	R94		0
3	5	R5		1	25	13	R11		2
16	6	R96		2	38	14	R90		3
17	7	R9		0	37	15	R14		1
50	16	R87	U2	5	70	24	R82	U8	6
49	17	R17		7	71	25	R23		4
62	18	R84		6	83	26	R26		5
63	19	R21		4	84	27	R78		7
46	20	R88		3	66	28	R83		0
45	21	R16		1	67	29	R22		2
58	22	R85		2	79	30	R25		1
59	23	R20		0	80	31	R79		3
174	32	R75	U4	5	195	40	R34	U7	0
173	33	R28		7	194	41	R70		2
187	34	R32		4	207	42	R37		3
186	35	R72		6	208	43	R66		1
170	36	R76		3	191	44	R33		6
169	37	R27		1	190	45	R71		4
183	38	R31		0	203	46	R36		5
182	39	R73		2	204	47	R67		7
216	48	R64	U5	5	237	56	R45	U6	6
215	49	R39		7	236	57	R59		4
228	50	R61		6	249	58	R48		5
229	51	R43		4	250	59	R55		7
211	52	R38		1	232	60	R60		0
212	53	R65		3	233	61	R44		2
224	54	R62		2	245	62	R47		1
225	55	R42		0	246	63	R56		3

First check the SPD data and EEPROM. Then check the following components for other problem.

	Clock loading	Boot failure
1-RANK	R77, RN2	SPD data, U3

15. Functional Diagram



16. PCB Specifications

General

1. Board size：69.6 x 30 mm ± 0.15 mm
2. Thickness：1.2 ± 0.1 mm
3. Pin count：260 PIN

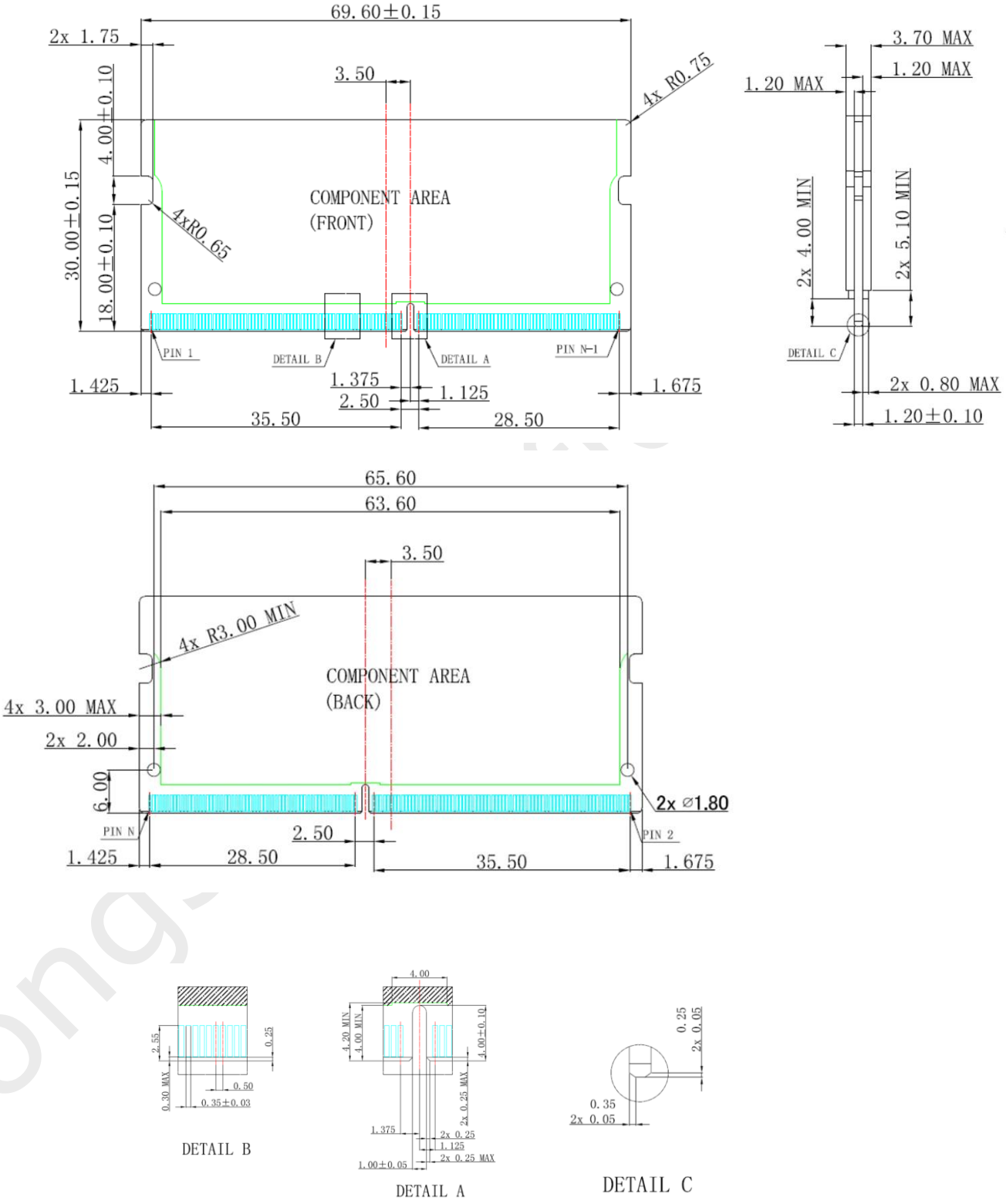
PCB Material

1. RoHS
2. Glass Epoxy FR4, .UL 94V-0, BP ML or BP 4M-1

Surface treatment:

1. Nickel Plating Thickness: 120 u” min.
2. Contact Pads Electrodeposited Gold Thickness: 3 u” min.

17. Module Dimensions



Units: millimeters