FORESEE 4GB DDR4 2666 SO-DIMM Datasheet

Version: 1.0

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Revision History

Revision No.	History	Draft Date	Remark
1.0	Release	Dec 2019	

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1. Description

FORESEE Unbuffered Small Outline DDR4 SDRAM DIMMs (Unbuffered Small Outine Double Data Rate Syn-chronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered Small Outline DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

2. Features

- VDD = VDDQ = 1.2V ±60mV
- VPP = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- 8 internal banks (x16): 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Nominal, park, and dynamic on-die termination(ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) capability

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3. Ordering Information

Part Number	Density	Speed	Component Composition	# of ranks
FD4AS2666C4GZE	4GB	DDR4 2666	512Mx16*4	1

4. Key Parameters

Grade	Speed (Mbps)	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
2666U	2666	0.750	18	13.5	13.5	32	45.5	18-18-18
2666V	2666	0.750	19	14.25	14.25	32	46.25	19-19-19

5. Address Table

	512*16
Number of Bank Groups	2
Bank group Address	BG0
Bank Address in a BG	BA[1:0]
Row Address	64K (A[15:0])
Column Address	1K (A[9:0])
Page size	2 KB

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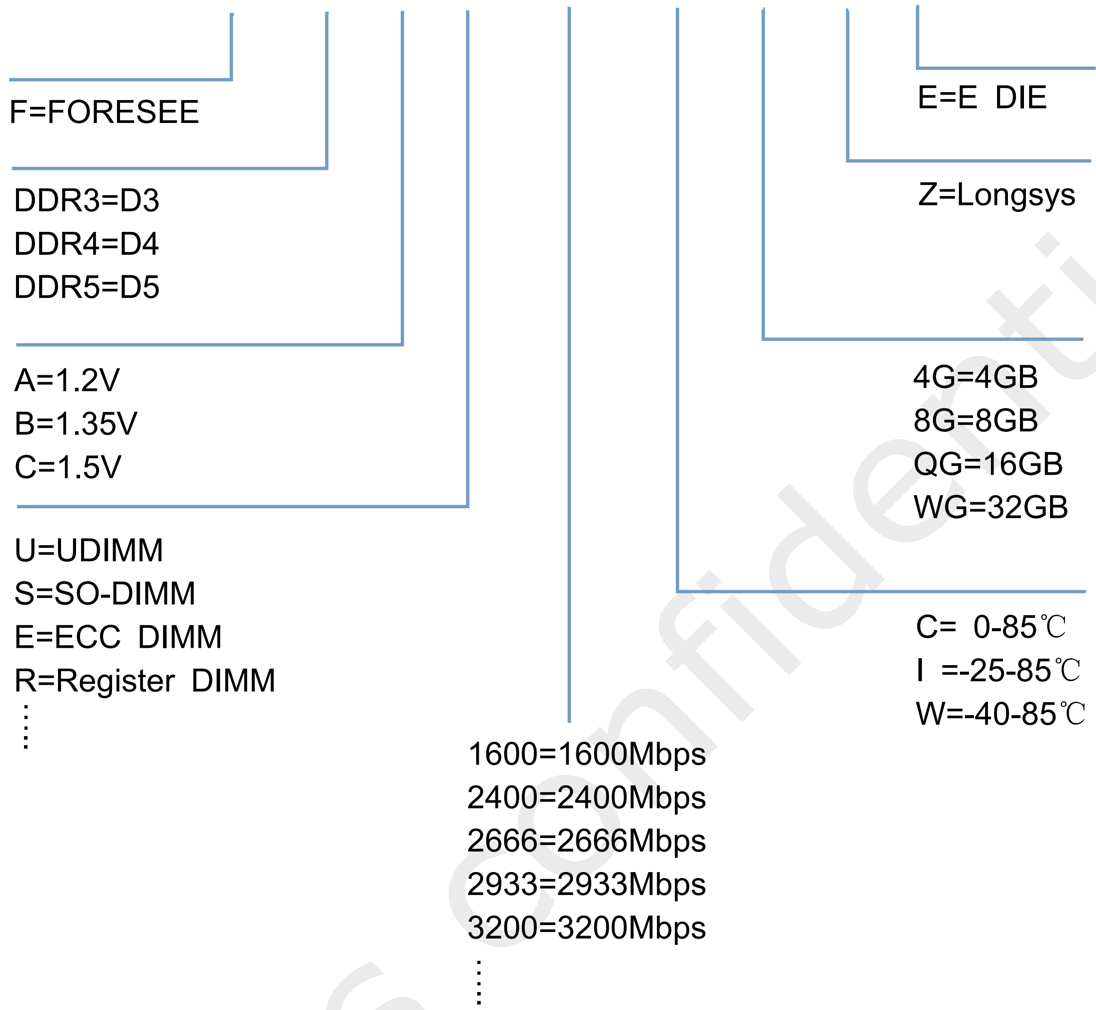

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6. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.

7. AC and DC Operating Conditions

Recommended Supply Operating Conditions

Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.14	1.2	1.26	V
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. VDD slew rate between 300mV and 80% of VDD,min shall be between 0.004 V/ms and 600V/ms, 20 MHz band-limited measurement.
4. VDD ramp time from 300mV to VDD,min shall be no longer than 200ms.

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8. 96-Ball FBGA – x16 Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQ8				UDQS_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DUQS_t	DQ9	VDD	B
C	VDDQ	DQ12	DQ10				DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQ14				DQ15	VSSQ	VDDQ	D
E	VSS	UDM_n/ UDBI_n	VSSQ				LDM_n/ LDBI_n	VSSQ	VSS	E
F	VSSQ	VDDQ	LDQS_c				DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	LDQS_t				VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6				DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/A14	ACT_n				CS_n	RAS_n/A16	VDD	L
M	VREFCA	BG0	A10/AP				A12/BC_n	CAS_n/A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

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9. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD/TS
RAS_n1	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n2	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n3	SDRAM write enable	VPP	SDRAM activating power supply
CSx_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)	VTT	mination supply for the Address, Com- mand and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Note 1 RAS_n is a multiplexed function with A16.

Note 2 CAS_n is a multiplexed function with A15.

Note 3 WE_n is a multiplexed function with A14.

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10. Input/Output Functional Descriptions

Symbol	Type	Function
CK0_t,CK0_c, CK1_t,CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self- Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID: Chip ID is only used for 3DS for 2 and 4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15, and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other command defined in command truth table.
DM_n/DBI_n	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying wherther to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.

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Symbol	Type	Function
BG0-BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components, only BG0 is valid.
BA0-BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input /Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c,	Input /Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
PARITY	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DSRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW.

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Symbol	Type	Function
ALERT_n	Output	ALERT: It has multiple functions, such as CRC error flag or Command and Address Parity error flag, as an Output signal. If there is an error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Use of this signal or not is dependent on the system.
SA0-SA1	Input	Device address for the SPD.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT[2]	Supply	Power Supply : 0.6V
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD.

Note:

1. For PC4, VDD 1.2V. For PC4L VDD is TBD.
2. For PC4, VTT is 0.6V. For PC4L VTT is TBD.

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11. Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VSS	2	VSS	131	A3	132	A2
3	DQ5	4	DQ4	133	A1	134	EVENT_n
5	VSS	6	VSS	135	VDD	136	VDD
7	DQ1	8	DQ0	137	CK0_t	138	CK1_t
9	VSS	10	VSS	139	CK0_c	140	CK1_C
11	DQS0_C	12	DM0_n, DBI0_n	141	VDD	142	VDD
13	DQS0_t	14	VSS	143	PARITY	144	A0
15	VSS	16	DQ6	KEY			
17	DQ7	18	VSS				
19	VSS	20	DQ2	145	BA1	146	A10/AP
21	DQ3	22	VSS	147	VDD	148	VDD
23	VSS	24	DQ12	149	CS0_n	150	BA0
25	DQ13	26	VSS	151	A14/WE_n	152	A16/RAS_n
27	VSS	28	DQ8	153	VDD	154	VDD
29	DQ9	30	VSS	155	ODT0	156	A15/CAS_n
31	VSS	32	DQS1_C	157	CS1_n	158	A13
33	DM1_n, DBI1_n	34	DQS1_t	159	VDD	160	VDD
35	VSS	36	VSS	161	ODT1	162	C0, CS2_n, NC
37	DQ15	38	DQ14	163	VDD	164	VREFCA
39	VSS	40	VSS	165	C1, CS3_n, NC	166	SA2
41	DQ10	42	DQ11	167	VSS	168	VSS
43	VSS	44	VSS	169	DQ37	170	DQ36
45	DQ21	46	DQ20	171	VSS	172	VSS
47	VSS	48	VSS	173	DQ33	174	DQ32
49	DQ17	50	DQ16	175	VSS	176	VSS
51	VSS	52	VSS	177	DQS4_C	178	DM4_n, DBI4_n
53	DQS2_c	54	DM2_n, DBI2_n	179	DQS4_t	180	VSS
55	DQS2_t	56	VSS	181	VSS	182	DQ39
57	VSS	58	DQ22	183	DQ38	184	VSS
59	DQ23	60	VSS	185	VSS	186	DQ35
61	VSS	62	DQ18	187	DQ34	188	VSS
63	DQ19	64	VSS	189	VSS	190	DQ45
65	VSS	66	DQ28	191	DQ44	192	VSS
67	DQ29	68	VSS	193	VSS	194	DQ41
69	VSS	70	DQ24	195	DQ40	196	VSS
71	DQ25	72	VSS	197	VSS	198	DQS5_c

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Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
73	VSS	74	DQS3_c	199	DM5_n, DBI5_n	200	DQS5_t
75	DM3_n, DBI3_n	76	DQS3_t	201	VSS	202	VSS
77	VSS	78	VSS	203	DQ46	204	DQ47
79	DQ30	80	DQ31	205	VSS	206	VSS
81	VSS	82	VSS	207	DQ42	208	DQ43
83	DQ26	84	DQ27	209	VSS	210	VSS
85	VSS	86	VSS	211	DQ52	212	DQ53
87	CB5, NC	88	CB4, NC	213	VSS	214	VSS
89	VSS	90	VSS	215	DQ49	216	DQ48
91	CB1, NC	92	CB0, NC	217	VSS	218	VSS
93	VSS	94	VSS	219	DQS6_C	220	DM6_n, DBI6_n
95	DQS8_c	96	DBI8_n	221	DQS6_t	222	VSS
97	DQS8_t	98	VSS	223	VSS	224	DQ54
99	VSS	100	CB6, NC	225	DQ55	226	VSS
101	CB2, NC	102	VSS	227	VSS	228	DQ50
103	VSS	104	CB7, NC	229	DQ51	230	VSS
105	CB3, NC	106	VSS	231	VSS	232	DQ60
107	VSS	108	RESET_n	233	DQ61	234	VSS
109	CKE0	110	CKE1	235	VSS	236	DQ57
111	VDD	112	VDD	237	DQ56	238	VSS
113	BG1	114	ACT_n	239	VSS	240	DQS7_c
115	BG0	116	ALERT_n	241	DM7_n, DBI7_n	242	DQS7_t
117	VDD	118	VDD	243	VSS	244	VSS
119	A12	120	A11	245	DQ62	246	DQ63
121	A9	122	A7	247	VSS	248	VSS
123	VDD	124	VDD	249	DQ58	250	DQ59
125	A8	126	A5	251	VSS	252	VSS
127	A6	128	A4	253	SCL	254	SDA
129	VDD	130	VDD	255	VDDSPD	256	SA0
				257	VPP	258	VTT
				259	VPP	260	SA1

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12. DDR4-2666 Speed Bins and Operations

Speed Bin		DDR4-2666U		Unit
CL-nRCD-nRP		18-18-18		
Parameter	Symbol	min	max	
Internal READ command to first data	tAA	13.5	18.00	ns
Internal READ command to first data with read DBI enabled	tAA_DBI	tAA(min) + 3nCK	-	ns
ACT to internal READ or WRITE delay time	tRCD	13.5	-	ns
PRE command period	tRP	13.5	-	ns
ACT to PRE command Period	tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period	tRC	tRAS + tRP	-	ns

Speed Bin		DDR4-2666V		Unit
CL-nRCD-nRP		19-19-19		
Parameter	Symbol	min	max	
Internal READ command to first data	tAA	14.25[5]	18.00	ns
Internal READ command to first data with read DBI enabled	tAA_DBI	tAA(MAX) + 3nCK	-	ns
ACT to internal READ or WRITE delay time	tRCD	14.25	-	ns
PRE command period	tRP	14.25	-	ns
ACT to PRE command Period	tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period	tRC	tRAS + tRP	-	ns

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13. Trouble shooting Guide

Description: DDRIV SDRAM, Single-Rank, x16-FBGA 96-Ball-based, x64 Unbuffered, 260-pin SO DIMM

Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ
8	0	4AR9(3-6)		DQL3	50	16	4AR11(3-6)		DQL3
7	1	4AR1(2-7)		DQL1	49	17	4AR3(2-7)		DQL1
20	2	2AR10(1-4)		DQL2	62	18	2AR12(1-4)		DQL2
21	3	2AR1(2-3)		DQL0	63	19	2AR3(2-3)		DQL0
4	4	4AR9(4-5)		DQL7	46	20	4AR11(4-5)		DQL7
3	5	4AR1(1-8)		DQL5	45	21	4AR3(1-8)		DQL5
16	6	2AR10(2-3)		DQL6	58	22	2AR12(2-3)		DQL6
17	7	2AR1(1-4)	U1	DQL4	59	23	2AR3(1-4)	U2	DQL4
28	8	2AR11(1-4)		DQU1	70	24	2AR13(1-4)		DQU1
29	9	2AR2(2-3)		DQU3	71	25	2AR4(2-3)		DQU3
41	10	4AR2(4-5)		DQU0	83	26	4AR4(4-5)		DQU0
42	11	4AR10(1-8)		DQU2	84	27	4AR12(1-8)		DQU2
24	12	2AR11(2-3)		DQU7	66	28	2AR13(2-3)		DQU7
25	13	2AR2(1-4)		DQU5	67	29	2AR4(1-4)		DQU5
38	14	4AR10(2-7)		DQU4	79	30	4AR4(3-6)		DQU4
37	15	4AR2(3-6)		DQU6	80	31	4AR12(2-7)		DQU6
174	32	4AR13(3-6)		DQL3	216	48	4AR15(3-6)		DQL3
173	33	4AR5(2-7)		DQL1	215	49	4AR7(2-7)		DQL1
187	34	2AR6(2-3)		DQL2	228	50	2AR16(1-4)		DQL2
186	35	2AR14(1-4)		DQL0	229	51	2AR8(2-3)		DQL0
170	36	4AR13(4-5)		DQL7	211	52	4AR7(1-8)		DQL7
169	37	4AR5(1-8)		DQL5	212	53	4AR15(4-5)		DQL5
183	38	2AR6(1-4)		DQL6	224	54	2AR16(2-3)		DQL6
182	39	2AR14(2-3)	U3	DQL4	225	55	2AR8(1-4)	U4	DQL4
195	40	2AR7(2-3)		DQU1	237	56	4AR8(2-7)		DQU1
194	41	2AR15(1-4)		DQU3	236	57	4AR16(3-6)		DQU3
207	42	4AR6(4-5)		DQU0	249	58	2AR17(2-3)		DQU0
208	43	4AR14(1-8)		DQU2	250	59	2AR9(1-4)		DQU2
191	44	2AR7(1-4)		DQU7	232	60	4AR16(4-5)		DQU7
190	45	2AR15(2-3)		DQU5	233	61	4AR8(1-8)		DQU5
203	46	4AR6(3-6)		DQU4	245	62	2AR9(1-4)		DQU4
204	47	4AR14(2-7)		DQU6	246	63	2AR17(2-3)		DQU6

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First check the SPD data and EEPROM. Then check the following components for other problem.

	Clock loading	Boot failure
1-RANK	R1, R3, R4	SPD data, TS1

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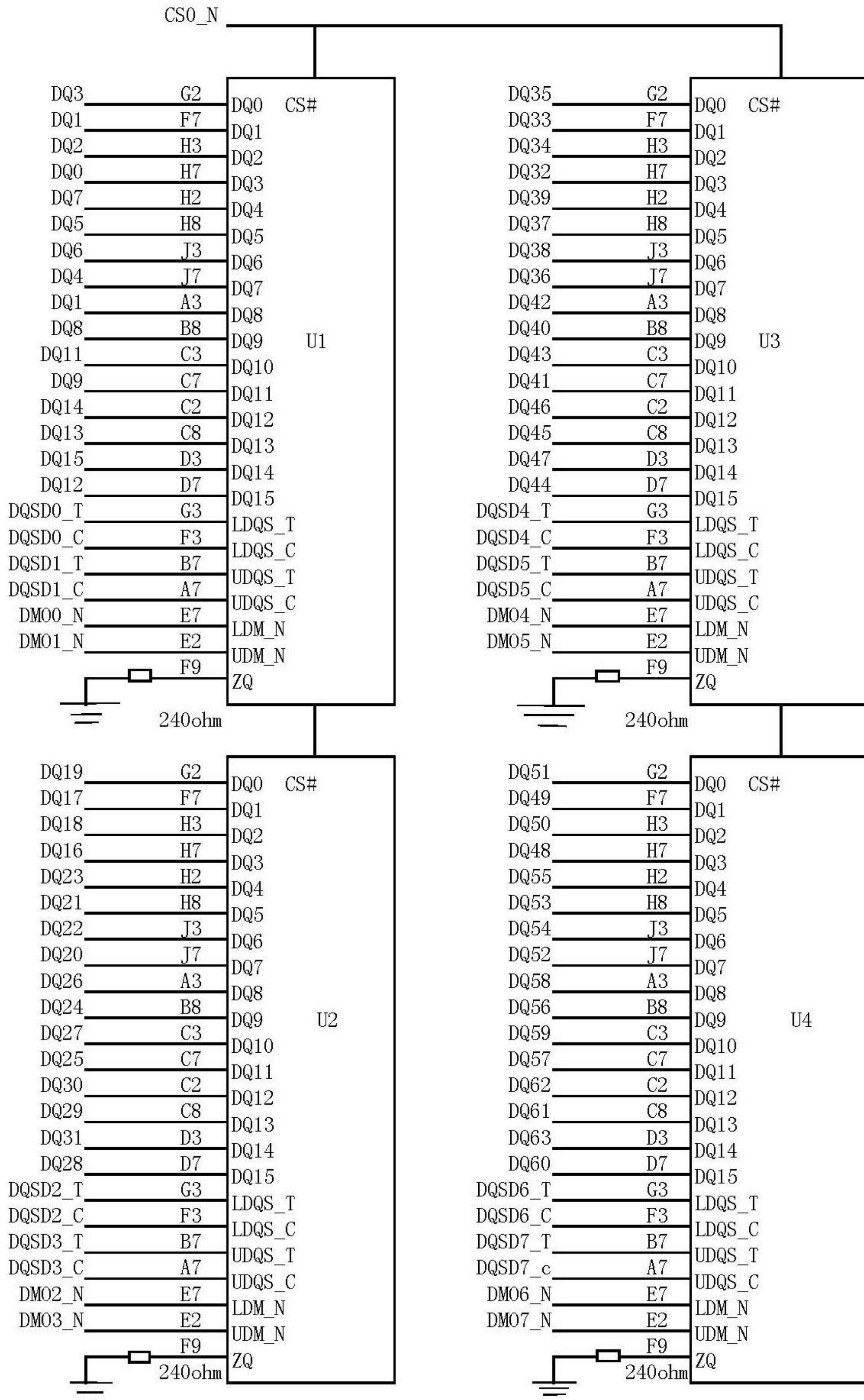
14. Functional Diagram



15. PCB Specifications

General

1. Board size：69.6 x 30 mm ± 0.15 mm
2. Thickness：1.2 ± 0.1 mm
3. Pin count：260 PIN

PCB Material

1. RoHS
2. Glass Epoxy FR4, .UL 94V-0, BP ML or BP 4M-1

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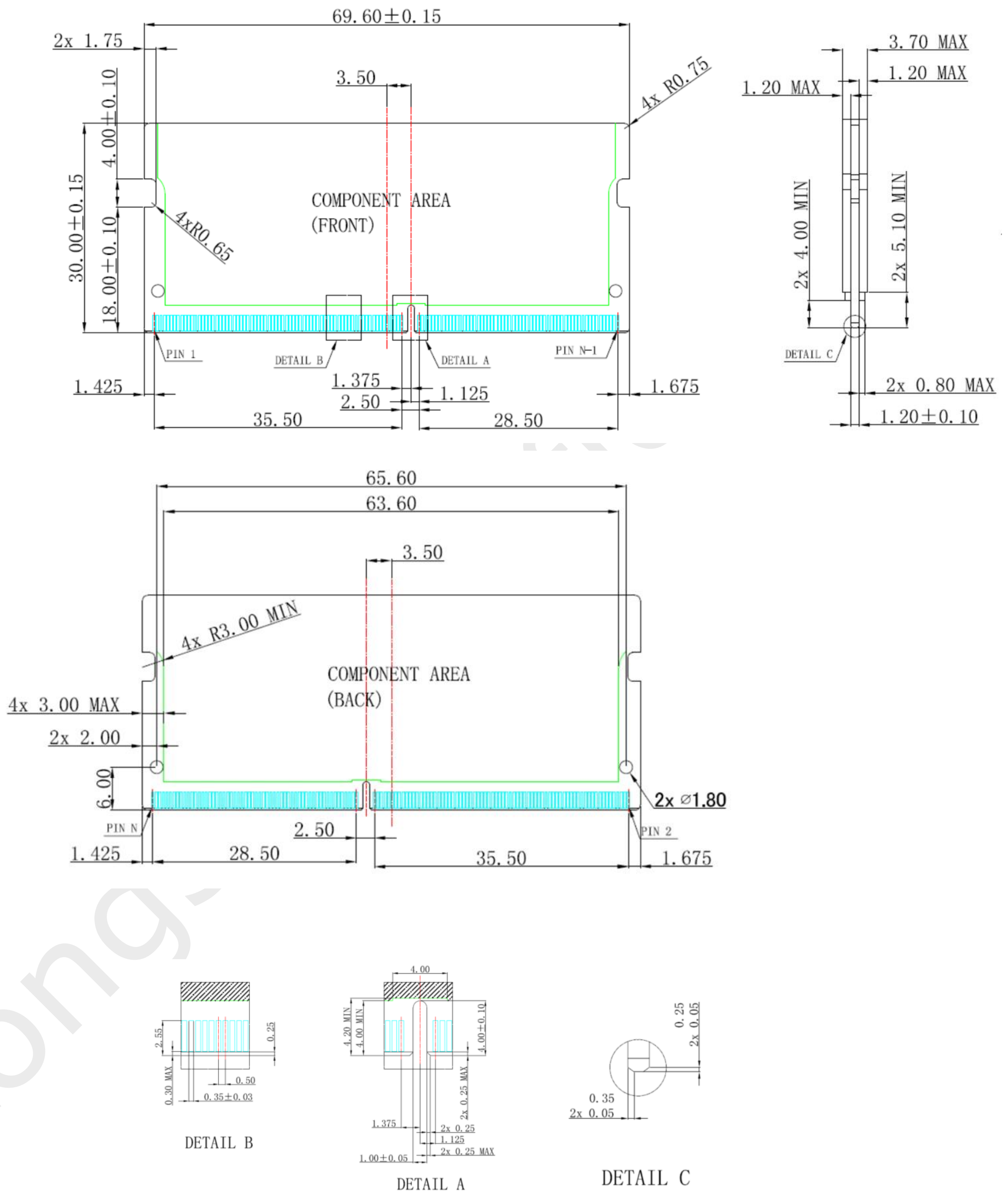
16. Module Dimensions



Units: millimeters